

RoHS Compliant
SATA Disk Chip Series
Datasheet for SDC
September 3, 2011
Revision 1.3



***This Specification Describes the Features and Capabilities of
the Standard and Industrial Temperature
SATA Disk Chip***

***Please Contact Fortasa Memory Systems Sales for any
Custom Features Required For Your Specific Application***



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Features:

- **Standard Serial SATA 2.5 (Gen. 2)**
 - SATA command set compatible
 - Serial SATA II –3.0 Gbps
 - ATA compatible command set
- **Low power consumption (typical)**
 - Supply voltage: 3.3V
 - Active mode: 300 mA
 - Sleep mode: 197 mA
- **Performance**
 - Burst transfer rate: 300 MB/sec
 - Sustained read: up to 53 MB/sec
 - Sustained write: up to 45 MB/sec
- **Capacity**
 - 1, 2, 4, 8 GB
- **NAND flash type: SLC**
- **Temperature ranges**
 - Operation:
 - Standard Temperature: 0 °C to 70 °C
 - Industrial Temperature: -40 °C to 85 °C
 - Storage: -40 °C to 100 °C
- **Intelligent endurance design**
 - Built-in hardware BCH ECC, correcting 8-bit or 15-bit error per 512-byte data sector
 - Global wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
 - Flash bad-block management
 - S.M.A.R.T. technology
- **Connector Type**
 - Standard 32/18 pin 600mil DIP
- **RoHS compliant**

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1 Product Description

1.1 General Description

Fortasa's SDC is a high-performance, SATA interface, solid state drive (SSD) designed to replace a conventional SATA hard disk drive. SDC supports standard SATA protocol and can be plugged into a standard SATA connector commonly found in rugged laptops, military devices, thin clients, Point of Sale (POS) terminals, telecom, medical instruments, surveillance systems and industrial PCs. Packaged in a 600 mil 32 or 18 round pin DIP package for easy and cost-effective mounting to a system motherboard, SDCs are designed to work at 3.3 Volts and use a standard SATA driver that is part of all major operating systems such as Microsoft's Windows series, Apple's MAC OS family, and UNIX variants.

The SDC offers capacities of up to 8 gigabytes, providing full support for the SATA II high-speed interface standard. It can operate at sustained access rates of up to 50 megabytes per second, which is much faster than other solid-state or traditional HDD SATA drives currently available on the market.

SDC offers high reliability global data wear-leveling scheme to allow uniform use of all storage blocks, increasing the lifetime of Flash media and optimizing drive performance. The SDC also offers Self-Monitoring Analysis and Reporting Technology (S.M.A.R.T.) feature that follows the SATA Rev. 2.5, ATA/ATAPI-7 specifications and uses the standard SMART command B0h to read data from the drive. This capability monitors the drive accesses and provides the host with vital information about drive condition to schedule maintenance and service times.

1.2 Functional Block

The SDC includes a single-chip SATA II Flash Controller and the flash media. The controller integrates the flash management unit with the controller itself to support multi-channel, multi-bank flash arrays. Figure 1-1 shows the functional block diagram.

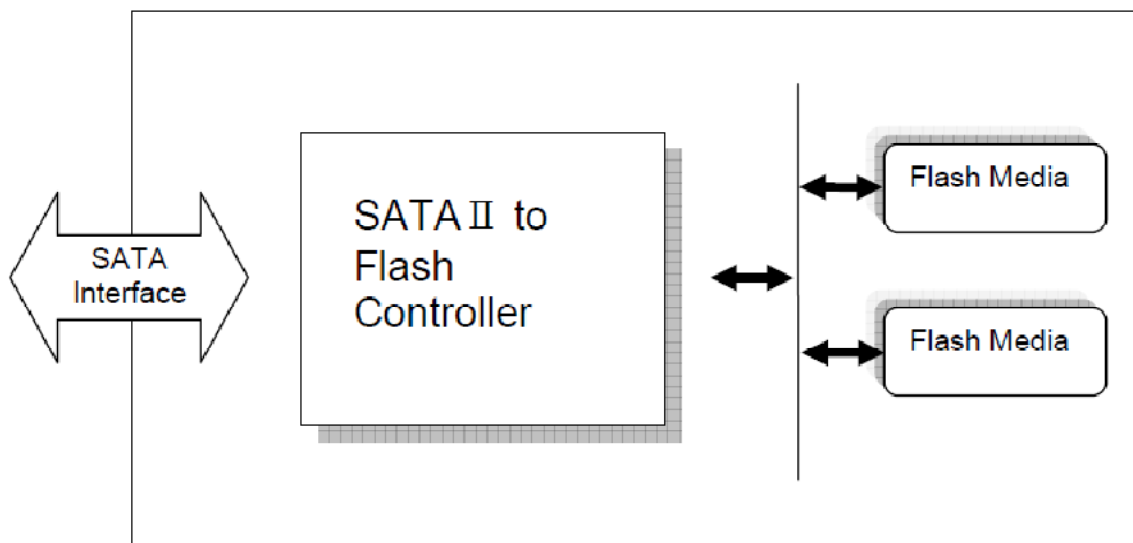


Figure 1-1: Functional block diagram

1.3 SATA Mode Support

The SATA-Disk Chip supports the following SATA operating modes:

- Supports up to PIO Mode-4
- Supports up to Multi-word DMA Mode-2
- Supports up to Ultra DMA Mode-5

1.4 Capacity Specification

Standard capacity specification of the SATA Disk Chip product is shown in Table 1-1. The table lists the specific capacity and the default numbers of heads, sectors and cylinders (CHS) for each product line.

Table 1-1: Capacity specifications

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
1GB	992,968,704	1,924	16	63	1,939,392
2GB	2,002,452,480	3,880	16	63	3,911,040
4GB	4,021,936,128	7,793	16	63	7,885,344
8GB	8,061,419,520	15,620	16	63	15,744,960

1. Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.

Please contact factory for any non-listed SATA Disk Chip capacity or custom CHS requirement.

1.5 Performance Specification

Performance of the SATA Disk Chip are listed in Table 1-2.

Table 1-2: Performance specifications

Capacity \ Performance	1GB	2GB	4 GB	8 GB
Sustained read (MB/s)	27	27	53	53
Sustained write (MB/s)	12	22	45	45

1.6 Pin Assignments

1.6.1 32 pins (16 x 2)

Figure 1-2: 32 Pin Package Pin-out

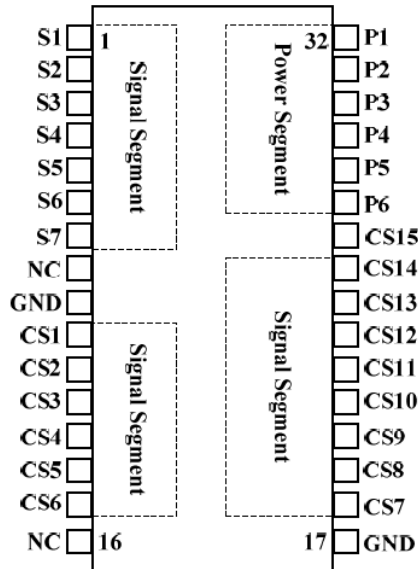


Table 1-3: Pin assignments for the 32-pin configuration

Pin No	Name	Type	Pin No	Name	Type
1	S1	GND	17	GND	GND
2	S2	RX+	18	CS7	Data Act.
3	S3	RX-	19	CS8	RS
4	S4	GND	20	CS9	RS
5	S5	TX-	21	CS10	RS
6	S6	TX+	22	CS11	RS
7	S7	GND	23	CS12	RS
8	NC		24	CS13	RS
9	GND	GND	25	CS14	RS
10	CS1	RS ¹	26	CS15	RS/WP
11	CS2	RS	27	P6	NA/UGND
12	CS3	RS	28	P5	NA/USB+
13	CS4	RS	29	P4	NA/USB-
14	CS5	RS	30	P3	NA/UVCC
15	CS6	PHY RDY	31	P2	GND
16	NC		32	P1	VCC3.3

1. RS: Reserved

1.6.2 18 pins (7x2 + 2x2)

Figure 1-3: 18 Pin Package Pin-out

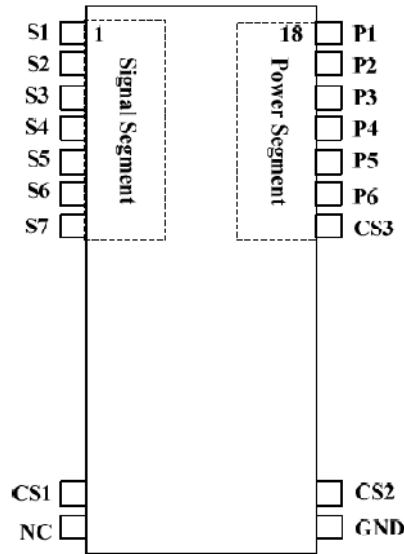


Table 1-4: Pin assignments for the 18-pin configuration

Pin No	Name	Type	Pin No	Name	Type
1	S1	GND	17	GND	GND
2	S2	RX+	18	CS2	Data Act
3	S3	RX-	19	CS3	RS ¹ /WP
4	S4	GND	20	P6	NA/UGND
5	S5	TX-	21	P5	NA/USB+
6	S6	TX+	22	P4	NA/USB-
7	S7	GND	23	P3	NA/UVCC
8	CS1	PHY RDY	24	P2	GND
9	NC	-	25	P1	VCC3.3

1. RS: Reserved

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 2-1: Command set

Command	Code	FR ¹	SC ²	SN ³	CY ⁴	DH ⁵	LBA ⁶
Check-Power-Mode	E5H	-	-	-	-	D8	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H	-	Y	-	-	D	-
Idle-Immediate	E1H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
Read DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H	-	-	-	-	D	-
Stand-By	E2H	-	-	-	-	D	-
Stand-By-Immediate	E0H	-	-	-	-	D	-
Write DMA	CAH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H	-	Y	Y	Y	Y	Y

1. FR - Features register

2. SC - Sector Count register

3. SN - Sector Number register

4. CY - Cylinder registers

5. DH - Drive/Head register

6. LBA - Logical Block Address mode supported (see command descriptions for use)

7. Y - The register contains a valid parameter for this command

8. For the Drive/Head register:

Y means both the SDC and Head parameters are used

D means only the SDC parameter is valid and not the Head parameter

2.1.1 Check-Power-Mode - E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command checks the power mode. Because the SATA Disk Chip can recover from sleep in 200ns, idle mode is never enabled. The SATA Disk Chip sets BSY, sets the Sector Count register to 00H, clears BSY and generates an interrupt.

2.1.2 Execute-Drive-Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command performs the internal diagnostic tests implemented by the SATA Disk Chip. If the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices, the Diagnostic codes shown in Table 2-2 are returned in the Error register at the end of the command.

Table 2-2: Diagnostic codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error

2.1.3 Flush-Cache - E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

2.1.4 Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

The Identify-Drive command enables the host to receive parameter information from the SATA Disk Chip. This command has the same protocol as the Read- Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 2-3. All reserved bits or words are zero. Table 2-3 is the definition for each field in the Identify-Drive Information.

Table 2-3: Identify-Drive information (1 of 3)

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0040H	2	General configuration bit-significant information
1	bbbbH ²	2	Default number of cylinders
2	C837H	2	Reserved
3	00bbH ²	2	Default number of heads
4-5	xxxxH	4	Reserved
6	bbbbH ²	2	Default number of sectors per track
7-8	bbbbH ²	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	000EH	2	Vendor Unique
10-19	ddddH ⁴	20	Unique serial number in ASCII
20	xxxxH	2	Retired
21	xxxxH	2	Retired
22	003FH	2	Obsolete
23-26	aaaaH ⁵	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	xxxxH	40	User Definable Model number/name
47	8000H	2	Maximum number of sectors on Read/Write-Multiple command
48	4000H	2	Reserved
49	2F00H	2	Capabilities
50	4000H	2	Reserved
51	0280H	2	PIO data transfer cycle timing mode
52	0000H	2	Obsolete
53	0007H	2	Translation parameters are valid

Table 1-3: Identify-Drive information (2 of 3)

Word Address	Default Value	Total Bytes	Data Field Type Information
54	nnnnH ³	2	Current numbers of cylinders
55	nnnnH ³	2	Current numbers of heads
56	nnnnH ³	2	Current sectors per track
57-58	nnnnH ³	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	0000H	2	Multiple sector setting
60-61	nnnnH ³	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Reserved
63	0007H	2	DMA data transfer is supported in SATA Disk Chip Controller
64	0003H	2	Advanced PIO Transfer Mode Supported
65	0078H	2	120ns cycle time support for Multiword DMA Mode-2
66	0078H	2	120ns cycle time support for Multiword DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	20	Reserved
80	01FEH	2	ATA/ATAPI major version number
81	0021H	2	ATA/ATAPI minor version number
82	0068H	2	Features/command sets supported
83	5000H	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85	0008H	6	Features/command sets Enabled
86	5000H	6	Features/command sets Enabled
87	4000H	6	Features/command sets Default
88	203FH	2	Ultra DMA Mode supported and selected
89	0000H	2	Time required for security erase unit completion
90	0000H	2	Time required for enhanced security erase unit completion

Table 2-3: Identify-Drive information (3 of 3)

Word Address	Default Value	Total Bytes	Data Field Type Information
91-127	0000H	74	Reserved
128	0001H	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-254	0000H	94	Reserved
255	0000H	2	Integrity Word

1. XXXX=This field is subject to change by the host or the device
 2. bbbb - default value set by controller. The selections could be user programmable.
 3. n - calculated data based on product configuration
 4. dddd - unique number of each device
 5. aaaa - any unique firmware revision
- The user has an option to change the model number during manufacturing.

1. Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, non-removable storage device with a transfer rate greater than 10 MB/sec and is not MFM encoded.

2. Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

3. Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

4. Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

5. Word 7-8: Reserved for assignment by CompactFlash Association

6. Word 10-19: Serial Number

Unique serial number ID. The twenty bytes are a user-programmable value with a default value of spaces.

7. Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

8. Word 27-46: Model Number

This field contains the model number for this product.

9. Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

10. Word 49: Capabilities

Bit	Function
13	Standby Timer 1: Standby timer values as specified in this standard are supported. 0: Standby timer values shall be managed by the device.
11	IORDY Supported 1: IORDY supported. 0: IORDY maybe supported.
10	IORDY Enabled 1: IORDY maybe disabled.
9	LBA Support 1: LBA mode addressing is supported.
8	DMA Support 1: DMA mode is supported.

11. Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. The SATA Disk Chip module supports up to PIO Mode-4

12. Word 53: Translation Parameters Valid

Bit	Function
0	1: Words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: Words 64-70 are valid to support PIO Mode-3 and 4.
2	1: Word 88 is valid to support Ultra DMA data transfer.

13. Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

14. Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

15. Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current numbers of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

16. Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the SATA Disk Chip in LBA mode only.

17. Word 63: Multiword DMA Transfer

This field identifies the Multiword DMA transfer modes supported by the SATA Disk Chip module and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time.

Bit	Function
15-11	Reserved
10	Multiword DMA mode-2 selected 1: Multiword DMA mode-2 is selected and bits 8 and 9 are cleared to 0. 0: Multiword DMA mode-2 is not selected.
9	Multiword DMA mode-1 selected 1: Multiword DMA mode-1 is selected and 8 and 10 shall be cleared to 0. 0: Multiword DMA mode-1 is not selected.
8	Multiword DMA mode-0 selected 1: Multiword DMA mode-0 is selected and bits 9 and 10 are cleared to 0. 0: Multiword DMA mode-0 is not selected.
7-3	Reserved
2	Multiword DMA mode-2 supported 1: Multiword DMA mode-2 and below are supported and Bits 0 and 1 shall be set to 1.
1	Multiword DMA mode-1 supported 1: Multiword DMA mode-1 and below are supported.
0	Multiword DMA mode-0 supported 1: Multiword DMA mode-0 is supported.

18. Word 64: Advanced PIO Data Transfer Mode

Bit (7:0) is defined as the PIO data and register transfer supported field. If this field is supported, Bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bit (7:2) are Reserved for future PIO modes.

Bit	Function
0	1: PIO Mode-3 is supported.
1	1: PIO Mode-4 is supported.

19. Word 65: Minimum Multiword DMA Transfer Cycle Time Per Word

This field defines the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the SATA Disk Chip supports when performing Multiword DMA transfers on a per word basis. The SATA Disk Chip supports up to Multiword DMA Mode-2, so this field is set to 120ns.

20. Word 66: Device Recommended Multiword DMA Cycle Time

This field defines the SATA Disk Chip recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the SATA Disk Chip may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. The SATA Disk Chip supports up to Multiword DMA Mode-2, so this field is set to 120ns.

21. Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The SATA Disk Chip minimum cycle time is 120ns. A value of 0078H is reported.

22. Word 68: Minimum PIO Transfer Cycle Time with IORDY

This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfer while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The SATA Disk Chip minimum cycle time is 120 ns, e.g., PIO mode 4. A value of 0078H is reported.

23. Word 80: Major Version Number

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since SATA standards maintain downward compatibility, a device may set more than one bit. The SATA Disk Chip supports ATA-1 to ATA-7.

24. Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the SATA-3 standard, word 81 shall be 0000H or FFFFH. A value of 0021H reported in word 81 indicates SATA/ATAPI-7 guided the implementation.

25. Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	1: Host Protected Area feature set is supported
9	1: Device Reset command is supported
8	1: Service interrupt is supported
7	1: Release interrupt is supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	1: Removable Media feature set is supported
1	1: Security Mode feature set is supported
0	1: SMART feature set is supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are not valid
14	1: Provides indications that the features/command sets supported words are valid
13-9	0: Reserved
8	1: Set-Max security extension supported
7	0: Reserved
6	1: SET FEATURES subcommand required to spin-up after power-up
5	1: Power-Up In Standby feature set supported
4	1: Removable Media Status feature set is supported
3	1: Advanced Power Management feature set is not supported
2	1: CFA feature set is not supported
1	1: Read DMA Queued and Write DMA Queued commands are supported
0	1: Download Microcode command is supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-2	0: Reserved
1	1: SMART self-test supported
0	1: SMART error logging supported

26. Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0: Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is not enabled
9	1: Device Reset command is enabled
8	1: Service interrupt is enabled
7	1: Release interrupt is enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	1: Removable Media feature set is enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	1: SMART feature set is enabled

Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension enabled
7-5	1: Reserved
4	1: Removable Media Status feature set is enabled
3	0: Advanced Power Management feature set is not enabled via the Set Features command 1: Advanced Power Management feature set is enabled via the Set Features command
2	1: CFA feature set is enabled
1	1: Read DMA Queued and Write DMA Queued commands are enabled
0	1: Download Microcode command is enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indications that the features/command sets supported words are valid
14	1: Provides indications that the features/command sets supported words are valid
13-2	0: Reserved
1	1: SMART self-test enabled
0	1: SMART error logging enabled

Word 88

Bit	Function
15-13	Reserved
12	1: Ultra DMA mode-4 is selected 0: Ultra DMA mode-4 is not selected
11	1: Ultra DMA mode-3 is selected 0: Ultra DMA mode-3 is not selected
10	1: Ultra DMA mode-2 is selected 0: Ultra DMA mode-2 is not selected
9	1: Ultra DMA mode-1 is selected 0: Ultra DMA mode-1 is not selected
8	1: Ultra DMA mode-0 is selected 0: Ultra DMA mode-0 is not selected
7-5	Reserved
4	1: Ultra DMA mode-4 and below are supported
3	1: Ultra DMA mode-3 and below are supported
2	1: Ultra DMA mode-2 and below are supported
1	1: Ultra DMA mode-1 and below are supported
0	1: Ultra DMA mode-0 is supported

27. Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value Not Specified
1-254	(Value * 2) minutes
255	>508 minutes

28. Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value Not Specified
1-254	(Value * 2) minutes
255	>508 minutes

29. Word 127: Removable Media Status Notification feature set support

Bit	Function
15-2	Reserved
1-0	00 Removable Media Status Notification feature set not supported
	01 Removable Media Status Notification feature set supported
	10 Reserved
	11 Reserved

30. Word 128: Security Status

Bit	Function
8	Security Level 1: Security mode is enabled and the security level is the maximum 0: Security mode is not enabled and the security level is the minimal
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked
1	Enable/Disable 1: Security is enabled
0	Capability 1: Supports security mode feature set

31. Word 255: Integrity Word

Bit	Function
15-8	Checksum
7-0	Signature

2.1.5 Idle - E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E3H							
C/D/H (6)		X		Drive			X	
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Timer Count (5msec increments)							
Feature (1)					X			

This command causes the SATA Disk Chip to set BSY, enter the Idle Mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero and the automatic power down mode is also enabled, the timer count is set to 3, with each count being 5ms. Note that this time base (5msec) is different from the ATA specification.

2.1.6 Idle-Immediate – E1H or 95H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E1H or 95H							
C/D/H (6)		X		Drive			X	
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the SATA Disk Chip to set BSY, enter the Idle Mode, clear BSY and generate an interrupt.

2.1.7 Initialize-Drive-Parameters – 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91H							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Number of Sectors			
Feature (1)					X			

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

2.1.8 Read DMA – C8H or C9H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C8H or C9H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)					Cylinder High (LBA 23-16)			
Cyl Low (4)					Cylinder Low (LBA 15-8)			
Sec Num (3)					Sector Number (LBA 7-0)			
Sec Cnt (2)					Sector Count			
Feature (1)					X			

This command executes in a similar manner to the READ SECTOR (S) command except for the following:

- The host initializes the DMA channel prior to issuing the command;
- Data transfers are qualified by DMARQ and are performed by the DMA channel;
- The SATA Disk Chip issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the DMA transfer phase of a READ DMA command, the SATA Disk Chip shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The flawed data is pending in the sector buffer. Subsequent sectors are transferred only if the error was a correctable data error. All other errors cause Read-DMA to stop after transfer of the sector that contained the error.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

2.1.9 Read-Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The Read- Multiple command is similar to the Read- Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set-Multiple command.

Command execution is identical to the Read- Sectors operation except that the numbers of sectors defined by a Set-Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Read-Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer.

The partial block transfer is for n sectors, where n = remainder (sector count/block count). If the Read-Multiple command is attempted before the Set-Multiple Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read-Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector counts of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

2.1.10 Read Sectors – 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sectors count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the SATA Disk Chip sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

2.1.11 Read Verify Sector(s) – 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read- Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the SATA Disk Chip sets BSY.

When the requested sectors have been verified, the SATA Disk Chip clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the Verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

2.1.12 Recalibrate – 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X	LBA	X	Drive			X	
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation command to the SATA Disk Chip and is provided for compatibility purposes.

2.1.13 Security-Disable-Password – F6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F6H							
C/D/H (6)		X		Drive			X	
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command requests a transfer of a single sector of data from the host. Table 2-5 defines the content of this sector of information. If the password selected by Word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 2-5: Security password data content

Word	Content
0	Control word: Bit 0: Identifier 0: Compare user password 1: Compare master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-256	Reserved

2.1.14 Security-Erase-Prepare – F3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

This command is issued immediately before the Security-Erase-Unit command to enable device erasing and unlocking. This command prevents accidental erasure of the data in the flash media.

2.1.15 Security-Erase-Unit – F4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F4H							
C/D/H (6)	X			Drive	X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

This command requests transfer of a single sector of data from the host. Table 2-5 defines the content of this sector of information. If the password does not match the password previously saved by the SATA Disk Chip, the SATA Disk Chip rejects the command with command aborted. The Security-Erase-Prepare command should be completed immediately prior to the Security-Erase-Unit command. If the SATA Disk Chip receives a Security-Erase-Unit command without an immediately prior Security-Erase-Prepare command, the SATA Disk Chip aborts the Security- Erase-Unit command.

2.1.16 Security-Freeze-Lock – F5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

The Security-Freeze-Lock command sets the SATA Disk Chip to Frozen mode. After command completion, any other commands that update the SATA Disk Chip Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security-Freeze-Lock is issued when the SATA Disk Chip is in Frozen mode, the command executes and the SATA Disk Chip remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0. Commands disabled by Security-Freeze-Lock are:

- Security-Set-Password
- Security-Unlock
- Security-Disable-Password
- Security-Erase-Unit

2.1.17 Security-Set-Password – F1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F1H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

This command requests a transfer of a single sector of data from the host. Table 2-5 defines the content of the sector of information. The data transferred controls the function of this command.

2.1.18 Security-Unlock – F2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F2H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					Config			
Feature (1)					Feature			

This command requests transfer of a single sector of data from the host. Table 2-6 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security-Unlock is issued and the device is locked. Once this counter reaches zero, the Security-Unlock and Security-Erase-Unit commands are command aborted until after a power-on reset or a hardware reset is received. Security-Unlock commands issued when the device is unlocked have no effect on the unlock counter.

Table 2-6: Identifier and security level bit interaction

Identifier	Level	Command Result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The SATA Disk Chip shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock mode shall be enabled from the next power-on reset or hardware reset. The SATA Disk Chip shall then be unlocked by only the User password. The Master password previously set is still stored in the SATA Disk Chip shall not be used to unlock the SATA Disk Chip.
User	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

2.1.19 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is effectively a NOP command to the SATA Disk Chip although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

2.1.20 Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 2-7 defines all features that are supported.

Table 2-7: Supported Features

Feature	Operation
02H	Enable write cache.
03H	Set transfer mode based on value in Sector Count register.
55H	Disable Read Look Ahead.
82H	Disable write cache.
AAH	Enable Read Look Ahead.

Features 02H and 82H allow the host to enable or disable write cache in the SATA Disk Chip that implements write cache. When the subcommand Disable-Write-Cache is issued, the SATA Disk Chip should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the SATA Disk Chip. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Table 2-6: Transfer mode values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode ¹
Multiword DMA mode	00100b	mode ¹
Ultra DMA mode	01000b	mode ¹
Reserved	Other	N/A

1. Mode = transfer mode number, all other values are not valid

2.1.21 Set-Multiple-Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)		X		Drive			X	
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the SATA Disk Chip to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the SATA Disk Chip sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted command error is posted, and Read- Multiple and Write- Multiple commands are disabled. If the Sector Count registers contains 0 when the command is issued, Read and Write- Multiple commands are disabled. At power-on, or after a hardware or (unless disabled by a Set-Feature command) software reset, the default mode is Read and Write-Multiple disabled.

2.1.22 Set-Sleep-Mode – E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E6H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the SATA Disk Chip to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

2.1.23 SMART – B0H

SMART Command signature is defined as cylinder being C2H to F4H. The feature register will indicate the subcommand as listed below. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

2.1.23.1 SMART Return Status – DAH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)					C2H			
Cyl Low (4)					4FH			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					DAH			

This Command is used to communicate the reliability status of the device to the host at the host's request. If the device has not detected a threshold exceeded condition, the device sets the LBA Mid register to 4FH and the LBA High register to C2H. If the device has detected a threshold exceeded condition, the device sets the LBA Mid register to F4H and the LBA High register to 2CH. In the current implementation, the only threshold checked is that if a fatal error has occurred.

2.1.23.2 SMART Enable/Disable Attribute Autosave – D2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	00H or F1H							
Feature (1)	D2H							

This command enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

2.1.23.3 SMART Enable Operations – D8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D8H							

Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameter.

2.1.23.4 SMART Disable Operations – D9H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D9H							

Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on. Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error. This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data is no longer be monitored or saved. The state of SMART is preserved across power cycles.

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2.1.23.5 SMART Execute Offline – D4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D4H							

This Command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and the save this data to the device’s memory. This data is not retained across resets and a new command must be executed to recollect data. The collected data should be read by a subsequent SMART Read Data (D0H) command.

2.1.23.6 SMART Read Data – D0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	D0H							

This Command returns the Device SMART data structure to the host. This command must be preceded by the SMART Execute Offline command with an appropriate subcommand listed above. The returned data will depend on the requested subcommand.

All returned data comply with the SMART data structure as specified in the SATA spec. Bytes 0 to 361 of the structure returns specific data that depends of the requested subcommand. Bytes 362 to 385 are standard values as defined in the ATA spec. bytes 386 to 510 returns specific data common to all subcommands. Byte 511 is the 2’s complement checksum of all bytes in the data structure.

Byte	Description
0-1	Data Structure Revision Number
2-13	1 st Attribute data
14-361	2 nd -30 th Individual Attribute Data
362	Off-line Data Collection Status
363	Reserved
364-365	Total Time in Seconds to Complete Off-line Data Collection
366	Reserved
367	Off-line Data Collection Capability
368-369	SMART Capability
370-510	Reserved
511	Data Structure Checksum

Byte 2-361: Individual Attribute Data

Byte	Description
0	Attribute ID
1-2	Status Flag (0x0002)
3	Attribute Value (0x64)
4-11	Vendor Specific

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ID	Description	Detail Information	
		Byte	Description
E5h	Halt System ID, Flash ID	0	Halt System ID
		1	Flash ID (byte 1)
		2	Flash ID (byte 2)
		3	Flash ID (byte 3)
		4	Flash ID (byte 4)
		5	Flash ID (byte 5)
		6	Flash ID (byte 6)
		7	Flash ID (byte 7)
E8h	Firmware version information	0	Year (High Byte, ASCII)
		1	Year (Low Byte, ASCII)
		2	Month (High Byte, ASCII)
		3	Month (Low Byte, ASCII)
		4	Day (High Byte, ASCII)
		5	Day (Low Byte, ASCII)
		6	Channels (binary)
		7	Banks (binary)
E9h	ECC Fail Record	0	ECC fail number
		1	Row address 3
		2	Row address 2
		3	Row address 1
		4	Channel number of last ECC fail
		5	Bank number of last ECC fail
		6	Reserved
		7	Reserved
EAh	Average Erase Count, Max Erase Count	0	Average Erase Count (High Byte)
		1	Average Erase Count
		2	Average Erase Count (Low Byte)
		3	Max Erase Count (High Byte)
		4	Max Erase Count
		5	Max Erase Count (Low Byte)
		6	Reserved
		7	Reserved
EBh	Good Block Count, System Block Count	0	Good Block Count (High Byte)
		1	Good Block Count
		2	Good Block Count (Low Byte)
		3	System(Free) Block Count (High Byte)
		4	System(Free) Block Count
		5	System(Free) Block Count (Low Byte)
		6	Reserved
		7	Reserved
ECh-FFh	Reserved		

Offline Data Collection Status (byte 362)

The offline data collection status byte indicates whether SMART data collection was successful or not. The host should check this value in the returned data structure before proceeding with interpretation of vendor specific data bytes. The follow are possible status values.

Value	Definition
00H	Offline data collection activity was never started.
02H	Offline data collection activity was completed without error.
04H	Offline data collection activity was suspended host.
05H	Offline data collection activity was aborted by host.
06H	Offline data collection activity was aborted by device.

2.1.23.7 SMART Enable/Disable Auto Off-line – DBH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	B0H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	C2H							
Cyl Low (4)	4FH							
Sec Num (3)	X							
Sec Cnt (2)	F8h or 00h							
Feature (1)	DBH							

Enables (when Sector Count register = “F8h”) or disables (Sector Count register = “00h”) the automatic off-line data collection function.

The automatic collection is disabled if a value of “00h” is set in the Sector Count register before a subcommand is issued. If automatic collection is disabled, the drive can still save attribute information during normal operation, such as during the power-on/off sequence or error correction sequence.

The automatic collection function is enabled if a value of “F8h” is set in the Sector Count register before the command is issued. Values other than “00h” and “F8h” are vendor-specific.

2.1.24 Standby – E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E2H							
C/D/H (6)	X		Drive		X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the SATA Disk Chip to set BSY, enter the Sleep mode (which corresponds to the SATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

2.1.25 Standby-Immediate – E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E0H							
C/D/H (6)		X		Drive			X	
Cyl High (5)					X			
Cyl Low (4)					X			
Sec Num (3)					X			
Sec Cnt (2)					X			
Feature (1)					X			

This command causes the SATA Disk Chip to set BSY, enter the Sleep mode (which corresponds to the SATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by simply issuing another command (a reset is not required).

2.1.26 Write-DMA – CAH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CAH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command executes in a similar manner to Write-RITE Sector(s) except for the following:

- The host initializes the DMA channel prior to issuing the command
- Data transfers are qualified by DMARQ and are performed by the DMA channel
- The SATA Disk Chip issues only one interrupt per command to indicate that data transfer has terminated and status is available.

During the execution of a Write-RITE DMA command, the SATA Disk Chip shall provide status of the BSY bit or the DRQ bit until the command is completed. At command completion, the command block registers contain the cylinder, head and sector number (LBA) of the last sector read.

If an error occurs after the attempted write of a transferred sector, the command is terminated and subsequent blocks are not transferred. The command block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors for successful completion of the command.

For Ultra-DMA mode, if a CRC error is detected during transfer, the ICRC and ABRT bits of the Error register are set at the end of the command.

2.1.27 Write-Multiple - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the SATA Disk Chip can support up to a block count of 1 as indicated in the Identify Drive Command information.

This command is similar to the Write-Sectors command. The SATA Disk Chip sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set-Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set-Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where: $n = \text{remainder}(\text{sector count/block count})$. If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

2.1.28 Write-Sector(s) - 30H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H							
C/D/H (6)	X	LBA	X	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

When this command is accepted, the SATA Disk Chip sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host. For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

2.2 Error Posting

The following table summarizes the valid status and error values for the ATA command set.

TABLE 2-7: Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				√		√	√	√		√
Execute-Drive-Diagnostic						√		√		√
Identify-Drive				√		√	√	√		√
Idle				√		√	√	√		√
Idle-Immediate				√		√	√	√		√
Initialize-Drive-Parameters						√		√		√
Read DMA	√	√	√	√	√	√	√	√	√	√
Read-Multiple	√	√	√	√	√	√	√	√	√	√
Read-Sector(s)	√	√	√	√	√	√	√	√	√	√
Read-Verify-Sector(s)	√	√	√	√	√	√	√	√	√	√
Recalibrate				√		√	√	√		√
Security-Disable-Password				√		√	√	√		√
Security-Erase-Prepare				√		√	√	√		√
Security-Erase-Unit				√		√	√	√		√
Security-Freeze-Lock				√		√	√	√		√
Security-Set-Password				√		√	√	√		√
Security-Unlock				√		√	√	√		√
Seek			√	√		√	√	√		√
Set-Features				√		√	√	√		√
Set-Multiple-Mode				√		√	√	√		√
Set-Sleep-Mode				√		√	√	√		√
SMART			√	√		√	√	√		√
Standby				√		√	√	√		√
Standby-Immediate				√		√	√	√		√
Write DMA	√		√	√	√	√	√	√		√
Write-Multiple	√		√	√	√	√	√	√		√
Write-Sector(s)	√		√	√	√	√	√	√		√
Invalid-Command-Code				√		√	√	√		√

√ = valid on this command

3. Flash Management

3.1 Error Correction/Detection

The SATA Disk Chip implements a hardware BCH-based ECC scheme to achieve up to 8/15 bit correction per 512-byte page.

3.2 Wear Leveling

All NAND flash devices are limited by a finite number of write cycles. Under a standard file system, frequent file table updates are mandatory. As a painful side effect of OS file overhead, some areas of flash address space wear out faster than others. As these certain sections get a substantially higher write occurrence the whole SATA Disk Chip can wear out very quickly. This uneven wear would significantly reduce the lifetime of the whole device, even if majority of the Flash sectors are far from the write cycle limit. Fortasa's SATA Disk Chip products offer advanced data wear leveling which distributes Flash writes evenly across the SATA Disk Chip memory space. By utilizing this advanced wear leveling feature, the lifetime of the media can be significantly extended.

3.3 Power Failure Management

The Low Power Detection on the Flash controller initiates cached data saving before the power supply to the device drops too low for operation. This feature prevents the device from system crash and ensures data integrity during an unexpected brownout. This feature makes sure that there are no catastrophic failures of the SATA Disk Chip due to system power glitches.

3.4 Quick Erase

Accomplished by the Secure Erase (SE) command, which added to the open ANSI standards that control disk drives, "Quick Erase" is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is a positive easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. The erase process will not stop until it is completed. In case of power failure, the erase process will continue when the power is reapplied to the device.

3.5 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Fortasa SMART feature follows the SATA Rev. 2.5, ATA/ATAPI-7 specifications, using the standard SMART command B0h to read data from the drive. And based on the SFF-8035i Rev. 2.0 specifications, Fortasa SMART defines 3 vendor-specified SMART Attribute IDs (E5h, E8h-EFh, and F3h) in the SATA Disk Chip products. They represent Flash ID, good block count, free-list block count, maximum erase count, average erase count, and firmware version information. When the Fortasa SMART Utility running on the host, it analyzes and reports the disk status to the host before the SATA Disk Chip is in critical condition.

4. Environmental Specifications

4.1 Environments

Environmental specification of the SATA Disk Chip series follows the MIL-STD-810F standard as shown in Table 4-1.

Table 4-1: Environmental specifications

Environment		Specification
Temperature	Operation	0°C to 70°C (Standard); -40°C to +85°C (Industrial)
	Storage	-40°C to 100°C
Vibration		Sine wave: 20~2000Hz, 16.3G (X, Y, Z axes)
Shock-Operating		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z; All 6 axes)
Humidity		5% to 95% RH (Non-condensing)

5. Electrical Specification

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

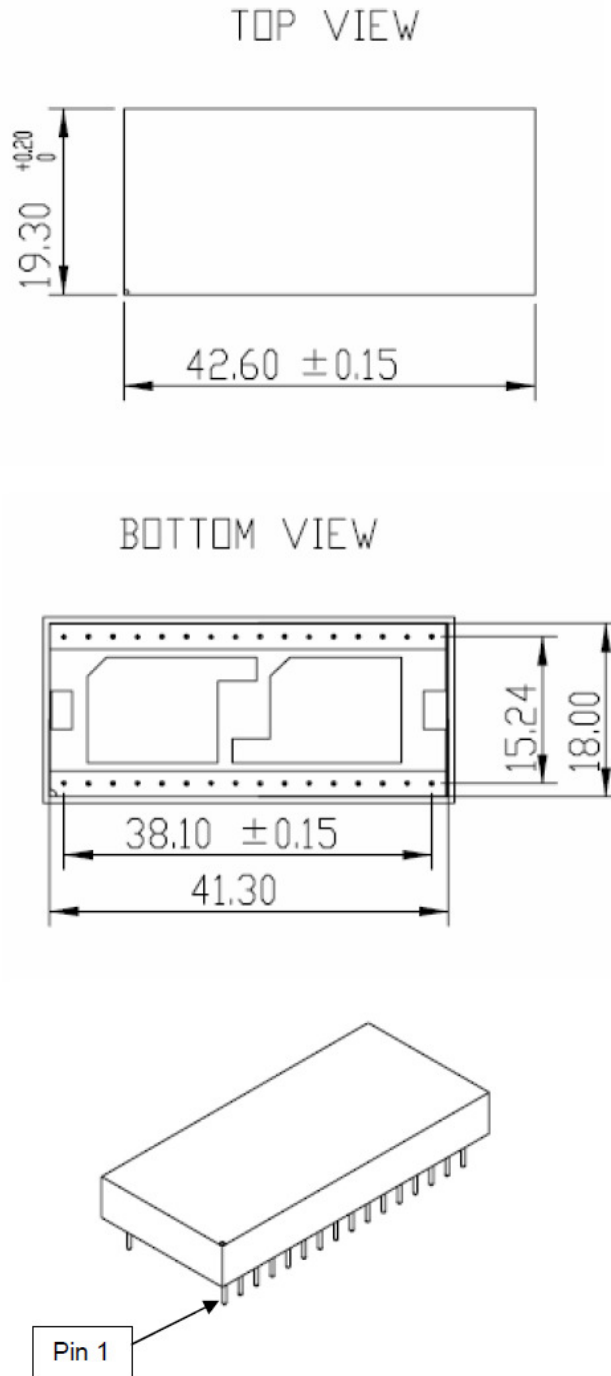
Table 5-1: Operating range

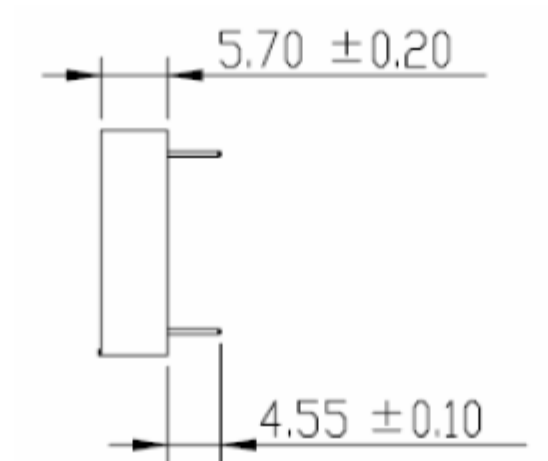
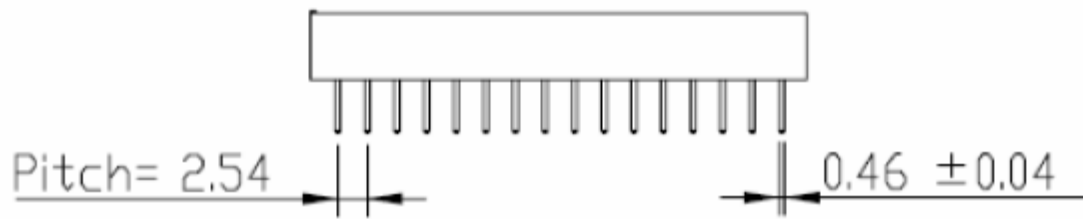
Range	Ambient Temperature	3V
Standard	0°C to +70°C	3.3-3.6V
Industrial	-40°C to +85°C	3.3-3.6V

6. Physical Characteristics

6.1 Dimensions of 32 pins (16x2)

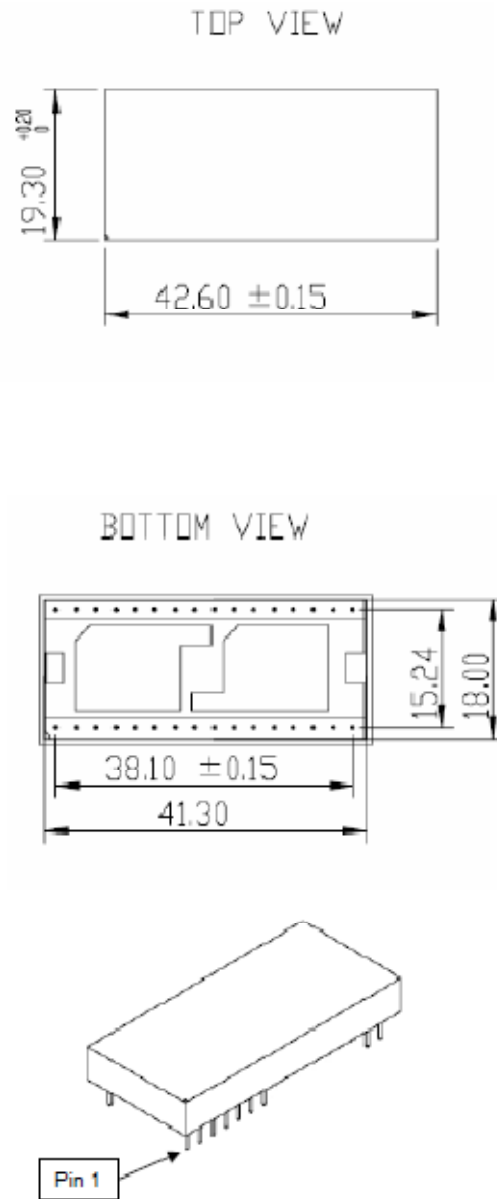
FIGURE 6-1: Physical dimensions of 32-pin SDC

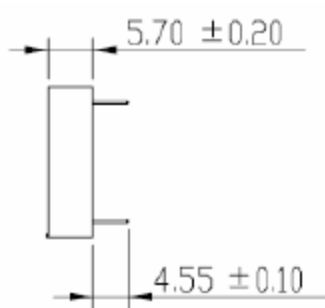
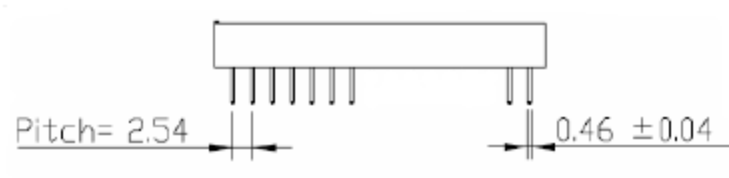




6.2 Dimensions of 18 pins (7x2 + 2x2)

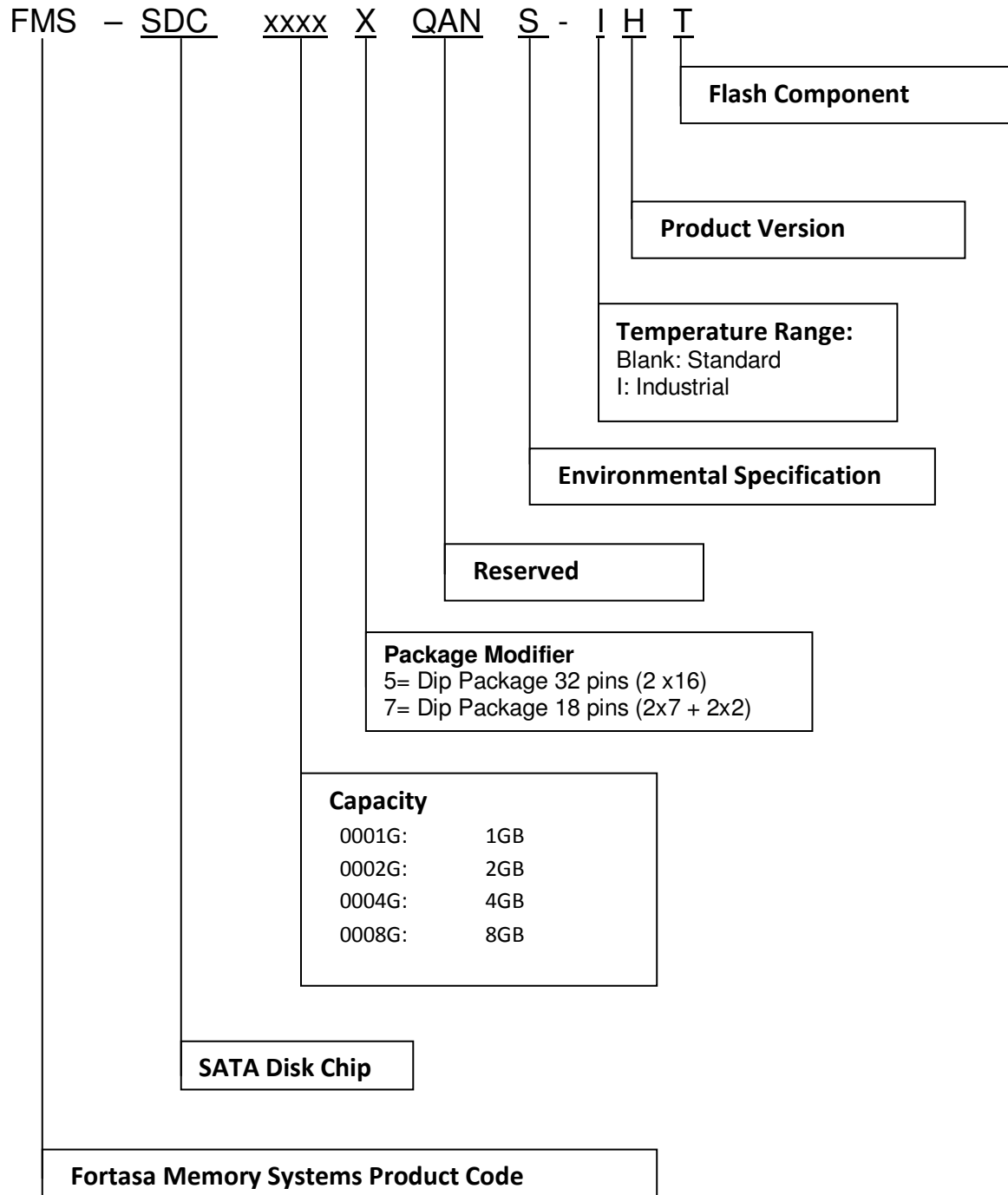
FIGURE 6-2: Physical dimensions of 18-pin SDC





7. Product Ordering Information

7.1 Product Code Designations



7.2 Valid Combinations

SDC 32 pin

Capacity	Standard Temperature	Industrial Temperature
1GB	FMS-SDC001G5QANS-HT	FMS-SDC001G5QANS-IHT
2GB	FMS-SDC002G5QANS-HT	FMS-SDC002G5QANS-IHT
4GB	FMS-SDC004G5QANS-HT	FMS-SDC004G5QANS-IHT
8GB	FMS-SDC008G5QANS-HT	FMS-SDC008G5QANS-IHT

SDC 18 pin

Capacity	Standard Temperature	Industrial Temperature
1GB	FMS-SDC001G7QANS-HT	FMS-SDC001G7QANS-IHT
2GB	FMS-SDC002G7QANS-HT	FMS-SDC002G7QANS-IHT
4GB	FMS-SDC004G7QANS-HT	FMS-SDC004G7QANS-IHT
8GB	FMS-SDC008G7QANS-HT	FMS-SDC008G7QANS-IHT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Fortasa sales representative to confirm availability of valid combinations and to determine availability of new product combinations

8. Revision History

Revision	Date	Description	Comments
1.0	8/1/2009	Initial Release	
1.1	3/18/2011	Modified Table 1-2, Changed Product Part Numbers	Switched from using Samsung 60nm SLC NAND to Toshiba 42nm SLC NAND
1.2	8/1/2011	Modified Table 1-3, Modified Table 5-1	Corrected pin definition for 32- pin device, Corrected 3.3V-only operating voltages
1.3	9/3/2011	Added Standard Temperature Part Numbers	