

RoHS Compliant

PCIe Gen 4x4 - M.2 - 2242 PCIe Flash Module Series

Datasheet for PCIe Gen 4x4 - M.2 2242 PCIe 3D TLC BICS5 NAND based Flash Module

February 2, 2023

Revision 1.0

This Specification Describes the Features and Capabilities of the Standard and Industrial Temperature M.2 PCIe Interface Modules

Please Contact Fortasa Memory Systems Sales for any Custom Features Required For Your Specific Application



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M.2 2242 PCle Flash Module

FMS-M24xxxx-xPEx



Endurance in (in TeraBytes Written: TBW)

86 TB

248 TB

661 TB

- 128 GB:

- 256 GB:

– 512 GB:

TCG OPAL 2.0 (Optional)

- 1024 GB: 1341 TB

- 2048 GB: 2876 TB

Features:

PCle Interface

- PCle Gen 4 x 4

Compliance

- NVMe 1.4

PCI Express Base 4.0

• Low power consumption (max)

Supply voltage: 3.3 ± 5%V

– Active mode: <5.5W</p>

Lilla and all districts

– Idle mode: <1.5W</pre>

NAND flash type: BICS5 - 3D NAND – TLC

• MTBF (hours): >1,500,000

Capacity

128GB, 256GB, 512GB, 1024GB, 2048GB

Temperature ranges

- Operation:

Standard: 0°C to 70°C Industrial: -40°C to 85°C

Storage: -40°C to 100°C

Performance

Sustained Performance

-Read: up to 3800 MB/sec -Write: up to 3300 MB/sec

Intelligent endurance design

- Built-in hardware LDPC based ECC algorithm
- Global wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
- Flash bad-block management
- Power Failure Management
- ATA Secure Erase
- SMART Command
- Trim Command

Connector Type

- 75-pin M.2 module pin-out

Form factor

- M.2 2242 PCIe Module Form Factor

Single Side: 80.00 x 22.00 x 2.15, unit: mmDouble Side: 80.00 x 22.00 x 3.50, unit: mm

Thermal Sensor for Temperature Management



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1 Product Description

1.1 General Description

Fortasa's M.2 PCIe 2242 Flash module is a high-performance, PCIe Gen 4 x 4 interface, solid state drive (SSD) designed to replace a conventional PCIe interface hard disk drive. This module supports industry standard PCIe protocol and can be plugged into a standard PCIe connector commonly found in rugged laptops, military devices, thin clients, Point of Sale (POS) terminals, telecom, medical instruments, surveillance systems and industrial PCs.

The M.2 PCIe 2242 module offers capacities of up to 2TB, providing full support for the PCIe high-speed interface standard. It can operate at sustained access rates of more than to 3800 megabytes per second, which is much faster than other solid-state or traditional HDD drives currently available on the market. Manufactured using TLC NAND-flash, this SSD offers cost effective solution to high capacity storage needs.

M.2 PCIe 2242 Flash Module offers high reliability global data wear-leveling scheme to allow uniform use of all storage blocks, increasing the lifetime of Flash media and optimizing drive performance. It also offers Self-Monitoring Analysis and Reporting Technology (S.M.A.R.T.) feature that follows the ATA/ATAPI specifications and uses the standard SMART command to read critical performance data from the drive. This capability monitors the drive accesses and provides the host with vital information about drive condition to schedule maintenance and service times.

1.2 Performance Specification

Performance of the M.2 PCIe 2242 Flash Module is listed in Table 1-1.

Table 1-1: Performance specifications

Performance Capacity	128GB	256GB	512GB	1024GB	2048GB
Sustained read (MB/s)	1100	2100	3800	3800	3400
Sustained write (MB/s)	1100	2000	3200	3300	3300
Random Read IOPS (4K)	110,000	200,000	450,000	700,000	600,000
Random Write IOPS (4K)	220,000	400,000	700,000	800,000	700,000

NOTES:

- 1. Adopts dynamic caching to deliver better performance and consumer user experience.
- 2. Performance may differ according to flash configuration, use condition, environment and platform.
- 3. Tested with CrystalDiskMark 7.0, QD32T1, 1GB range.
 - IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned
- 4. Performance specification is under Thermal Throttling inactivated.
- 5. Operating System: Windows 10 Professional (x64); Intel Core i7-8700K CPU @ 3.70GHz
- $6. \ Measurement\ environment:\ Room\ temperature:\ 20^{\sim}25^{\circ}C,\ humidity:\ 40^{\sim}60\%RH,\ DC+3.3V\ condition.$



1.3 Pin Assignments

This connector does not support hot plug capability. There is a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into both Key B and Key M connectors.

TOP VIEW

M

Pin 1

Figure 1-1: M.2 PCle connectors

Table 1-4: Signal Segment

Pin	Signal	Description
1	GND	CONFIG_3 = GND
2	3.3V	Supply Pin, 3.3V
3	GND	Ground
4	3.3V	Supply Pin, 3.3V
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	No Connect	No Connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	No Connect	No Connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	Supply Pin, 3.3V
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	Supply Pin, 3.3V
15	GND	Ground
16	3.3V	Supply Pin, 3.3V
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	Supply Pin, 3.3V



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19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec	
20	No Connect	No Connect	
21	GND	Ground	
22	No Connect	No Connect	
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec	
24	No Connect	No Connect	
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec	
26	No Connect	No Connect	
27	GND	Ground	
28	No Connect	No Connect	
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec	
30	No Connect	No Connect	
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec	
32	No Connect	No Connect	
33	GND	Ground	
34	No Connect	No Connect	
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec	
36	No Connect	No Connect	
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec	
38	No Connect	No Connect	
39	GND	Ground	
40	SMB_CLK	CMP. Clask. Onen Dusin with mill we are platforms	
40	(I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform	
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec	
42	SMB_DATA	SMBus Data; Open Drain with pull-up on platform	
	(I/O)(0/1.8V)		
43	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec	
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low	
45	GND	Ground	
46	No Connect	No Connect	
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec	
48	No Connect	No Connect	
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec	
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification	
51	GND	Ground	
	CLKREQ#(I/O)(0/3.3	Clock Request is a reference clock request signal as defined by the	
52	V)	PCIe Mini CEM specification; Also used by L1 PM Sub-states	
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express	
		M.2 spec	
54	PEWAKE#(I/O)(0/3. 3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low	



55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec	
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.	
57	GND	Ground	
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.	
59	CONFIG_2	Defines module type	
60	Module Key M		
61	Module Key M		
62	Module Key M		
63	Module Key M	Module Key	
64	Module Key M		
65	Module Key M		
66	Module Key M		
67	No Connect	No Connect	
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module	
69	No Connect	PEDET (NC-PCIe)	
70	3.3V	Supply Pin, 3.3V	
71	GND	Ground	
72	3.3V	Supply Pin, 3.3V	
73	GND	Ground	
74	3.3V	Supply Pin, 3.3V	
75	GND	Ground	



2. Software Interface

2.1 Command Set

Table 2-1 summarizes the M.2 PCle 2242 command set.

Table 2-1 Admin Commands

Opcode	Command Description	Supported
00h	Delete I/O Submission Queue	Supported
01h	Create I/O Submission Queue	Supported
02h	Get Log Page	Supported
04h	Delete I/O Completion Queue	Supported
05h	Create I/O Completion Queue	Supported
06h	Identify	Supported
08h	Abort	Supported
09h	Set Features	Supported
0Ah	Get Features	Supported
0Ch	Asynchronous Event Request	Supported
10h	Firmware Activate	Supported
11h	Firmware Image Download	Supported
14h	Device Self Test	Supported
80h	Format NVM	Supported
81h	Security Send	Supported
82h	Security Receive	Supported
84h	Sanitize	Supported

Table 2-3 NVM Commands

Opcode	Command Description	Supported
00h	Flush	Supported
01h	Write	Supported
02h	Read	Supported
04h	Write Uncorrectable	Not Supported
05h	Compare	Supported
08h	Write Zeroes	Supported
09h	Dataset Management	Supported



2.2 S.M.A.R.T. Technology

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved



SMART Parameters (Log Identifier C0h)

Byte	Length in Bytes	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	ECC Fail Count
262-273	12	Reserved
274-277	4	Total Later Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase Count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-511	210	Reserved

3. Flash Management

3.1 Error Correction/Detection

The M.2 PCIe 2242 implements a hardware LDPC (Low Density Parity Check) ECC algorithm.

3.2 Wear Leveling

All NAND flash devices are limited by a finite number of write cycles. Under a standard file system, frequent file table updates are mandatory. As a painful side effect of OS file overhead, some areas of flash address space wear out faster than others. As these certain sections get a substantially higher write occurrence the whole Flash Drive can wear out very quickly. This uneven wear would significantly reduce the lifetime of the whole device, even if majority of the Flash sectors are far from the write cycle limit. Fortasa's M.2 PCle 2242 Flash Drive products offer advanced data wear leveling which distributes Flash writes evenly across the Flash Drive memory space. By utilizing this advanced wear leveling feature, the lifetime of the media can be significantly extended.

3.3 Power Failure Management

The Low Power Detection on the Flash controller initiates cached data saving before the power supply to the device drops too low for operation. This feature prevents the device from system crash and ensures data integrity during an unexpected brownout. This feature makes sure that there are no catastrophic failures of the Flash Drive due to system power glitches.

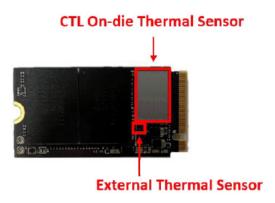
3.4 TRIM Command Support

Over time the performance of SSD degrades as user continually writes and erases data. The TRIM command "formats" the SSD to optimize the drive performance. A TRIM enabled SSD running an OS with TRIM support will stay closer to its peak performance without much performance variance.



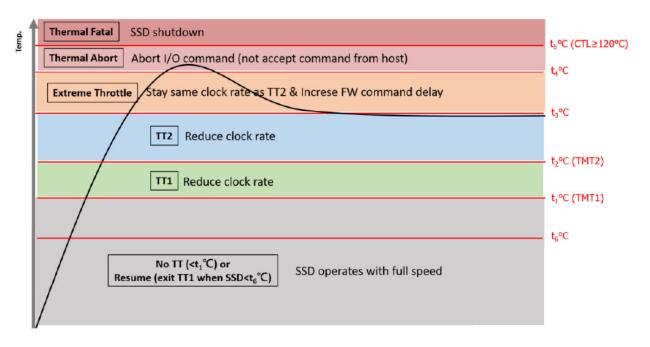
3.5 Thermal Sensor

The M.2 PCIe 2242 SSD contains an on-die (embedded into Flash Controller) and off-die (Separate Component) Thermal Sensors that measure module and Flash Controller temperatures. The module temperature can also be obtained by polling SMART Command attribute ID 194 (0xC2). When the device temperature reaches a pre-set temperature threshold, the module performance will be reduced to limit the power draw and prevent the module from overheating.



3.6 Thermal Throttling

Based on the measurement of the Thermal Sensor M.2 PCIe 2242 SSD adjusts the drive performance to reduce the heat generation and cool the drive. When the device temperature reaches a pre-set temperature threshold, the module performance will be reduced to limit the power draw and prevent the module from overheating. After the drive temperature measurement drop below the pre-set temperature value the drive performance will adjust back to the maximum level.





Default Thermal Throttling Temperature Settings

	Stage	Status	Operation temperature
$t_1//t_6$	No TT / Resume	SSD Operates at Full Speed	<82°C / <74°C
t ₁	TT1	Reduce Clock Rate	82°C
t 2	TT2	Reduce More Clock Rate	78°C
t 3	Extreme Throttle	Same Clock Rate as TT2 &	95°C
	(TT Protect)	Increase FW command delay	
t ₄	Thermal Abort	Abort I/O command (not accept I/O	98°C
		command from host)	
t 5	Thermal Fatal	SSD shutdown	100°C
			(or CTL≥120°C)

3.7 TCG OPAL 2.0 (Optional)

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

TCG Opal 2.0 Main Features:

- AES 256-bitHardware Self Encryption
- Deploy Storage Device & Take Ownership: The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device: LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device: unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life: erasure of data

3.8 Read Only Mode (End of Life)

When drive becomes severely aged by repeated program/erase cycles, the spare block count will be reduced. When the number of usable good (spare) blocks falls below a defined threshold, the drive will notify Host through SMART read status command with an advanced Warning for the drive to enter Read Only Mode to prevent further data corruption. User should check SMART data frequently to identify drive end of life warning to gracefully replace the overused drive.



4. Environmental Specifications

4.1 Environments

Environmental specification of the M.2 PCIe 2242 Flash Drive series follows the MIL-STD-810F standard as shown in Table 4-1.

Table 4-1: Environmental specifications

Environment		Specification
Tomoroturo	Operation	0°C to 70°C (Standard); -40°C to 85°C (Industrial)
Temperature Storage		-40°C to +85°C
Vibration		Non-Operating: 20Hz~80Hz/1.52mm, 80Hz~2000Hz/20G
Shock		Non-operating: 1500 G, 0.5 ms
Humidity		RH 90% under 40°C

4.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in the M.2 PCIe 2242 drive. Based on provided component data, M.2 PCIe 2242 Flash Drive is rated at more than 1,500,000 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on "Telcordia Technologies Special Report, SR-332, Issue 2" method.

4.3 Endurance

The endurance of a storage device is predicted by a JEDEC approved test methodology. The data, reported in TeraBytes Written (TBW), is based on several factors related to device architecture and product usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Please contact Sales to learn more about the TBW analysis and calculations.

Capacity	TBW
128GB	86
256GB	246
512GB	661
1024GB	1341
2048GB	2876

Notes:

- 1. TBW is measured by JEDEC Client 219A workload and calculated with PE count = 3000.
- 2. TBW may differ according to flash configuration and platform configuration.
- 3. The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Certain Windows OS, Linux kernel version before 2.6.33, other OS please reference the respective OS user manual)
- 4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor..



5. Electrical Specification

5.1 Operating Voltage

Caution: Absolute Maximum Stress Ratings – Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 5-1: Operating range

Range	Ambient Temperature	3.3V
Standard	0°C to +70°C	3.3V ±5%
Industrial	-40°C to +85°C	3.3V ±3/6

5.2 Power Consumption

Tables 5-2 lists the M.2 PCIe 2242 power consumption.

Table 5-2 M.2 PCIe 2242 power consumption

Capacity Performance	128GB	256GB	512GB	1024GB	2048GB
Active Mode (W) (typical)	2.9	4.2	5.2	5.3	4.2
Idle Mode (mW) (max)			1,500		

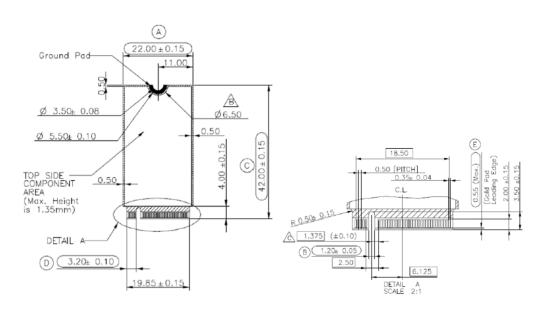
Notes:

- 1. Use CrystalDiskMark 7.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
- 2. The measured power voltage of M.2 2242 SSD is 3.3V.
- 3. Power consumption may differ according to flash configuration, use condition, environment and platform.
- 4. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

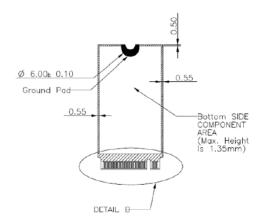


6. Physical Characteristics

6.1 Dimensions



Top View

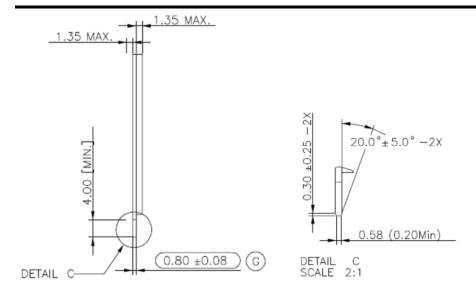


Bottom View

M.2 2242 PCIe Flash Module

FMS-M24xxxx-xPEx





Side View

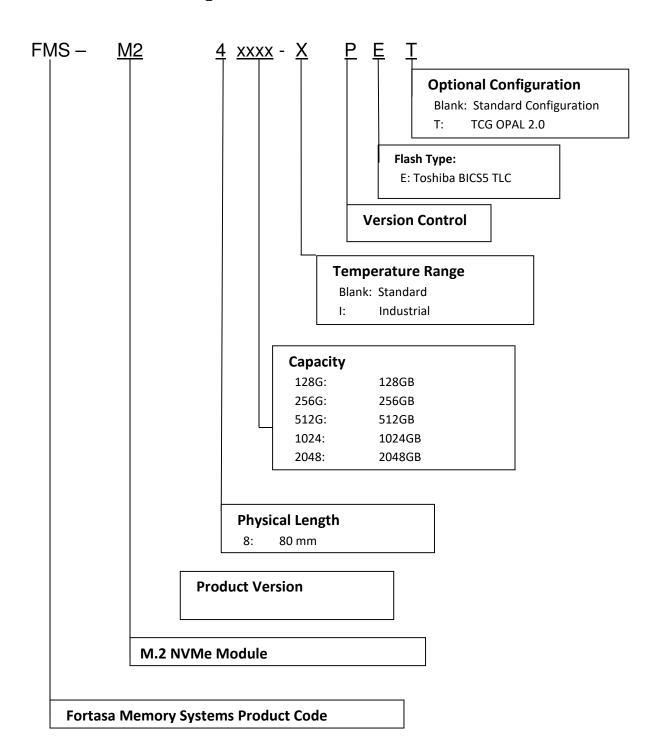
Notes:

- Max Component Height
 Max Component
 Max Component
 Signal Vias / Signal Copper / Printing
- 4.General Tolerance \pm 0.15mm
- 5. are critical dimensions



7. Product Ordering Information

7.1 Product Code Designations





7.2 Valid Combinations

Capacity	Standard Temperature Model Numbers	Industrial Temperature Model Numbers
128GB	FMS-M24128G-PE	FMS-M24128G-IPE
256GB	FMS-M24256G-PE	FMS-M24256G-IPE
512GB	FMS-M24512G-PE	FMS-M24512G-IPE
1024GB	FMS-M241024-PE	FMS-M241024-IPE
2048GB	FMS-M242048-PE	FMS-M242048-IPE

TCG OPAL 2.0 Enabled

Capacity	Standard Temperature Model Numbers	Industrial Temperature Model Numbers
128GB	FMS-M24128G-PET	FMS-M24128G-IPET
256GB	FMS-M24256G-PET	FMS-M24256G-IPET
512GB	FMS-M24512G-PET	FMS-M24512G-IPET
1024GB	FMS-M241024-PET	FMS-M241024-IPET
2048GB	FMS-M242048-PET	FMS-M242048-IPET

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Fortasa sales representative to confirm availability of valid combinations and to determine availability of new product combinations



8. Revision History

Revision	Date	Description	Comments
1.0	2/2/2023	Initial Release	

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