RoHS Compliant

Industrial ATA PCMCIA Series

February 6, 2014
Revision 1.2

This Specification Describes the Features and Capabilities of the Standard and Industrial Temperature PCMCIA Cards

Please Contact Fortasa Sales for any Custom Features Required For Your Specific Application

4151 Middlefield Road
2nd Floor
Palo Alto, CA 94303 USA
888-367-8588
www.fortasa.com

Features:

- **PCMCIA Association Specification Standard Interface**
  - PC Card Memory Mode
  - PC Card I/O Mode
  - TrueIDE Mode
    - PIO Mode-6
    - Multiword DMA Mode-4
    - Ultra DMA Mode-6
- **Connector Type**
  - 68 pin connector Type II form factor
- **Low power consumption**

  5.0V Operation
  - Write active mode: 28 mA (typ) / 30 mA (max)
  - Read active mode: 23 mA (typ) / 30 mA (max)
  - Sleep mode: 0.2 mA (max)

  3.3V Operation
  - Write active mode: 28 mA (typ) / 30 mA (max)
  - Read active mode: 23 mA (typ) / 30 mA (max)
  - Sleep mode: 0.2 mA (max)
- **Performance**
  - Sustained read: Up to 35.0 MBytes/s in UDMA mode 6
  - Sustained write: Up to 28.0 MBytes/s in UDMA mode 6
- **Capacity**

  128, 256, 512 MB
  1, 2, 4, 8, 16 GB
- **NAND flash type: SLC**
- **Superior Reliability Through Built-in Hardware ECC**
  - Corrects up to 4-symbols per 512-byte sector
- **Temperature ranges**
  - Operation:

    Standard Temperature: 0°C to 70°C
    Industrial Temperature: -40°C to 85°C
  - Storage: -55°C to 125°C
- **Dimensions: Type II form factor: 85.6mm(L) x 54.0mm(W) x 5.03mm(H)**
- **MTBF > 4,000,000 hours**
- **High shock & vibration tolerance**
- **Less than 1 Error in 10^{14} bits read**
- **W/E Endurance: 4,000,000 write/erase cycles**
- **RoHS compliant**

Table of Contents

1. General Description

Fortasa's Industrial PCMCIA Card (PC) offers the highest reliability and performance storage solution critical to most demanding OEM customers. Unlike off-the-shelf consumer Flash cards, Fortasa's Industrial PC card offers superior manufacturing quality and component traceability to ensure all that product shipments match that of a qualified product.

Fortasa's PC card provides complete PCMCIA - ATA functionality and compatibility. Fortasa 's PC Card technology is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications. Featuring advanced technologies such as Advanced Wear-leveling algorithms and Built-in Hardware ECC, Fortasa's Industrial PC Card offers the most reliable storage solution for most critical applications.

Offered in both standard and industrial temperature ranges, Fortasa's Industrial PC card product should be the most trustworthy solution in the OEM memory system.

2. Functional Block

The PCMCIA Card includes a controller and flash media, as well as the PCMCIA standard interface. Figure 2-1 shows the functional block diagram.

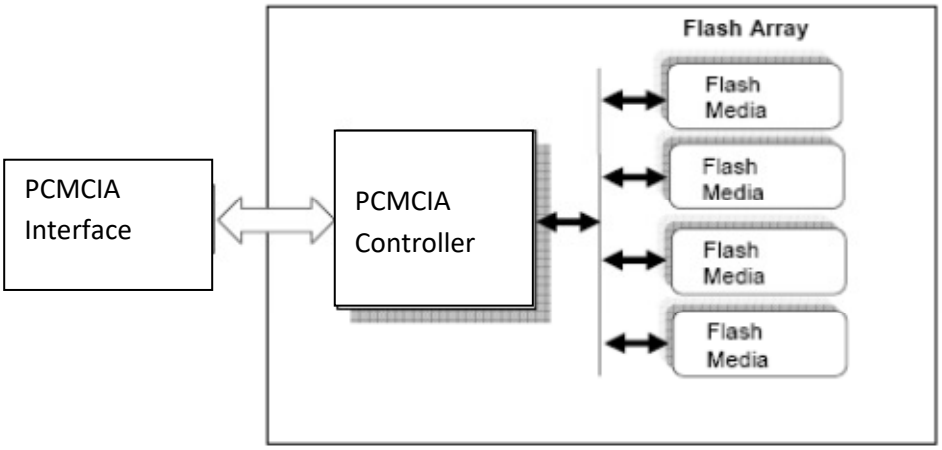


Figure 2-1: Functional block diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 68-pin configuration. A "+" suffix indicates the active low signal. The pin type can be input, output or input/output.

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin Number	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
1	GND		GND		GND	
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	CE1#	I	CE1#	I	CE1#	I
8	A10	I	A10	I	A10	I
9	OE#	I	OE#	I	ATASEL#	I
10	N.C.	-	N.C.	-	N.C.	-
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	N.C.	-	N.C.	-	N.C.	-
14	N.C.	-	N.C.	-	N.C.	-
15	WE#	I	WE#	I	WE#	I
16	RDY/BSY	O	IREQ#	O	INTRQ	O
17	Vcc		Vcc		Vcc	
18	N.C.	-	N.C.	-	N.C.	-
19	N.C.	-	N.C.	-	N.C.	-
20	N.C.	-	N.C.	-	N.C.	-
21	N.C.	-	N.C.	-	N.C.	-
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	IOIS16#	O	IOIS16#	O
34	GND		GND		GND	

	Memory card mode		I/O Card Mode		True IDE Mode	
Pin Number	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
35	GND		GND		GND	
36	CD1#	O	CD1#	O	CD1#	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I	D15	I	D15	I
42	CE2#	I	CE2#	I	CE2#	I
43	VS1	O	VS1	O	VS1	O
44	IORD#	I	IORD#	I	IORD#	I
45	IOWR#	I	IOWR#	I	IOWR#	I
46	NC	-	NC	-	NC	-
47	NC	-	NC	-	NC	-
48	NC	-	NC	-	NC	-
49	NC	-	NC	-	NC	-
50	NC	-	NC	-	NC	-
51	Vcc		Vcc		Vcc	
52	NC	-	NC	-	NC	-
53	NC	-	NC	-	NC	-
54	NC	-	NC	-	NC	-
55	NC	-	NC	-	NC	-
56	CSEL#	I	CSEL#	I	CSEL#	I
57	VS2	O	VS2	O	VS2	O
58	RESET	I	RESET	I	RESET#	I
59	Wait#	O	Wait#	O	IORDY	O
60	INPACK#	O	INPACK#	O	INPACK#	O
61	REG#	I	REG#	I	REG#	I
62	BVD2	I/O	SPKR#	I/O	DASP	I/O
63	BVD1	I/O	STSCHG#	I/O	PDIAG#	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	O	D10	O	D10	O
67	CD2#	O	CD2#	O	CD2#	O
68	GND		GND		GND	

Notes:
1) CD1# and CD2# are grounded internal to PC Card

3.1 Signal Description

Symbol	Type	Name and Function
A0 – A10	INPUT	**ADDRESS INPUTS:** A0 through A10 Signal A0 is not used in word access mode. A10 is the most significant bit. In True IDE Mode only HA[2..0] are used for selecting the eight registers in the Task File, the remaining address lines should be grounded.
D0 - D15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** D0 THROUGH D15 constitute the bi-directional databus. D0 - D7 constitute the lower (even) byte and D8 - D15 the upper (odd) byte. D15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** active low signals; CE1# enables even byte accesses, CE2# enables odd byte accesses. In True IDE Mode CE2# is used to select the Alternate Status Register and the Device control Register while CE1# is the cheap select for the other task file registers.
OE#, ASTEL#	INPUT	**OUTPUT ENABLE, ATA Select:** Active low signal enabling read data from Attribute and Common memory area. To enable True IDE Mode this input should be grounded by the host.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card. In true IDE Mode this input signal is not used and should be connected to Vcc.
RDY/BSY# IREQ# INTRQ	OUTPUT	**Ready/Busy, Interrupt Request:** In I/O mode this signal is is IREQ# pin. The signal of low level indicates that the card is requesting software service to host, and high level indicate that the card is not requesting. In memory mode, the signal is set high when the ATA card is ready to accept new data transfer operation and held low when card is busy. At power up and at Reset, the RDY/BSY is low until (busy) until the card has completed its power up or reset function. Host should provide a pull up resistor
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP IOIS16#	OUTPUT	**Write Protect, 16 bit I/O port:** In memory mode, WP is held low: always writable). In I/O mode , IOIS16# is asserted low when Task File Registers are accessed in 16 bit mode. In True IDE mOde this signal is asserted low when this device is expecting a word data transfer cycle.
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** No Connection for ATA card.
VCC		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND:** for all internal circuitry.
REG#	INPUT	**ATTRIBUTE MEMORY SELECT:** Used to enable access to Attribute space. Should be in high level during common memory area access. In True IDE Mode input signal is not used and should be connected to Vcc.
Reset Reset#	INPUT	**Reset, Reset#:** Active signal will clear all registers on the card (power on default). In True IDE Mode Reset# is the active low hardware reset from the host.

Symbol	Type	Name and Function
WAIT#	OUTPUT	**WAIT:** This signal outputs low level for purpose of delaying memory or I/O access cycle. In True IDE Mode this signal can be used as IORDY.
BVD2 SPKR# DASP#	Input/Output	**Battery Voltage Detect 2, Data audio output, Disk active/slave present:** In memory card mode, BVD2 is always high. In I/O mode, SPKR# is held high: no digital audio signals. In True IDE Mode DASP# is Disk Active/Slave Present signal in Master/Slave handshake protocol.
BVD1 STSCHNG# PDIAG#	Input/Output	**Battery Voltage Detect 1, Status Change, Pass Diagnostic:** In memory card mode BVD1 Is set to high level. In I/O mode STSCHNG# is used to alert the host to changes in Status registers. In True IDE mode PDIG is the Pass Diagnostic signal in Master/Slave handshake protocol.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V, 16 bit card has been inserted.
CSEL#	Input	**Card Select:** This signal is not used in memory and I/O mode. With internal pull up resistor this signal is used to configure this card as Master or Slave when configured in True IDE Mode. When this pin is GND, selected Master config, when pin is open the card is configured as a Slave.
INPACK#	Output	**Input Acknowledge**: This signal is not used in memory mode. It is asserted by the card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used for the input data buffer control. In True IDE Mode this signal is not used and should not be connected at the host.
IORD#	Input	**I/O Read:** is used for control of read data in Task File area. This card respond to this signal only in I/O interface mode
IOWR#	Input	**I/O Write:** is used for control of data write in Task File area. This card respond to this signal only in I/O interface mode

4. Capacity Specification

Standard capacity specification of the PCMCIA Card products are shown in Table 4-1. The table lists the specific capacity and the default numbers of heads, sectors and cylinders (CHS) for each product line.

Table 4-1: Capacity specifications

Capacity	Total Bytes[1,2]	Cylinders	Heads	Sectors	Max LBA
256MB	256,901,120	980	16	32	501,760
512MB	512,483,328	993	16	63	1,000,944
1GB	1,024,966,656	1,986	16	63	2,001,888
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,097,802,240	7,940	16	63	8,003,520
8GB	8,195,604,480	15,880	16	63	16,007,040

1. Total bytes includes reserved system blocks.
2. Total bytes displayed varies depending on the operating system.

Please contact Fortasa Memory System Sales for any non-listed PCMCIA Card capacity or custom CHS requirement.

4.1 Performance Specification

Performance of the PCMCIA Card are listed in Table 4-2.

Table 4-2: PC Card Performance specification

Item	Performance (PIO mode 4 true IDE)
Read Transfer Rate	(Typical) Up to 35MB/s
Write Transfer Rate	(Typical) Up to 28 MB/s
Burst Transfer Rate	Up to 40MB/s
Controller Overhead (Command to DRQ)	1ms typical, 5ms (max)

4.2 Reliability Specification

Reliability specification of the PCMCIA Card are listed in Table 4-3.

Table 4-3: PC Card reliability specification

Item	Value
MTBF(@25°C)	> 4,000,000 Hours
Data Reliability	< 1 Non-Recoverable Error in 10^{14} Bits Read
Endurance	> 4,000,000 write/erase cycles

4.3 Environmental Specifications

Environmental specification of the PCMCIA Card series follows the MIL-STD-810F standard as shown in Table 4-4.

Table 4-4: Environmental specifications

Environment		Specification
Temperature	Operation	JEDEC - JESD STD A104 Temp condition N (-40°C to 85 °C) and soak mode 3; 200 cycles
	Storage	-55°C to 125°C
Vibration		Method 514.5, procedure 1, category 24, 1 hour per axis
Shock		Method 516.5, procedure 1, non-operational, 40g, SRS functional shock for ground equipment, three (3) shock per axis (positive or negative) JEDEC- JESD22-B, 104A, test condition B, 1500g pulse, 0.5 msec
Humidity		Method 507.4, Paragraph 4.5.2 - 10 day test per figure 507.4-1, 10 day test
Altitude		Method 500.4, procedure II, modified to 80,000 ft and nonoperation 1 hr test duration at altitude.

5. Flash Management

The most critical attribute of an Industrial grade PCMCIA Card is its inherent high level of reliability. This characteristic is achieved through unique technical features of Flash Controller and specific component selection that offer higher degree of reliability compared to the consumer grade components.

5.1 Intelligent Flash Controller Features

5.1.1 Advanced wear-leveling algorithms

All NAND flash devices are limited by a finite number of write cycles. Under a standard file system, frequent file table updates are mandatory. As a painful side effect of OS file overhead, some areas of flash address space wear out faster than others. As these certain sections get a substantially higher write occurrence the whole PCMCIA card can wear out very quickly. This uneven wear would significantly reduce the lifetime of the whole device, even if majority of the Flash sectors are far from the write cycle limit. Fortasa's PCMCIA Card products offer advanced data wear leveling which distributes Flash writes evenly across the card memory space. By utilizing this advanced wear leveling feature, the lifetime of the media can be significantly extended.

5.1.2 Built-in hardware ECC

The Fortasa Flash Controller uses superior Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to four symbols of errors for each 512-byte block of data. High performance is achieved through hardware-based error detection and correction.

6. Identify Drive Information

Table 6-1: Identify-Drive information (1 of 2)

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH[1]	2	General configuration bit-significant information
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track.
5	0240H	2	Number of unformatted bytes per sector.
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[2]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-19	ddddH[4]	20	Unique serial number in ASCII
20	0002H	2	Buffer type
21	0002H	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write-Long-Sector Commands
23-26	aaaaH[5]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[6]	40	User Definable Model number/name
47	0001H	2	Maximum 1 sector on Read/Write-Multiple command
48	0000H	2	Reserved
49	0300H	2	Capabilities: DMA Supported (bit 8), LBA supported (bit 9).
50	0000H	2	Reserved
51	0203H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0003H	2	Translation parameters are valid
54	nnnnH[3]	2	Current numbers of cylinders
55	nnnnH[3]	2	Current numbers of heads
56	nnnnH[3]	2	Current sectors per track
57-58	nnnnH[3]	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010xH	2	Multiple sector setting
60-61	nnnnH[3]	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Reserved
63	0407H	2	DMA data transfer is supported in ATA Flash Disk Controller
64	0003H	2	Advanced PIO Transfer Mode Supported

Table 6-2: Identify-Drive information (1 of 2)

Word Address	Default Value	Total Bytes	Data Field Type Information
65	0078H	2	120ns cycle time support for Multiword DMA Mode-2
66	0078H	2	120ns cycle time support for Multiword DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-127	0000H	130	Reserved
128-159	0000H	64	Reserved vendor unique bytes.
159-255	0000H	192	Reserved

1. CompactFlash and PCMCIA cards in True IDE mode report 044AH
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. dddd - unique number of each device
5. aaaa - any unique firmware revision
6. cccc - default value is "xxxMB PCMCIA card" where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

7. Electrical Specification

Caution: **Absolute Maximum Stress Ratings –** Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1: Operating range

Range	Ambient Temperature	3.3V	5V
Commercial	0°C to +70°C	3.135-3.465V	4.75-5.25V
Industrial	-40°C to +85°C		

Table 7-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V_{cc}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to GND	V	-0.5V min to V_{cc} + 0.3V max

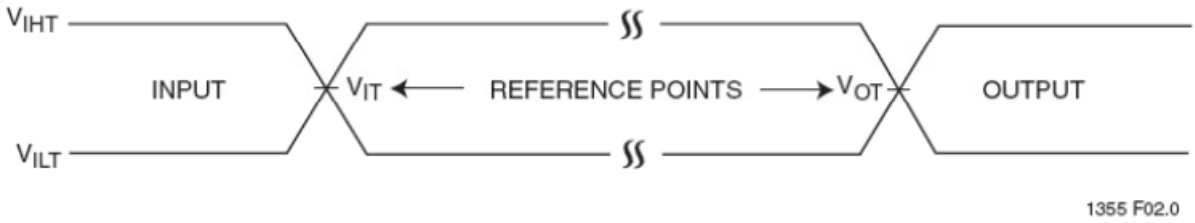
7.1 DC Characteristics

Table 7-3: DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input LOW Voltage	-0.30	0.80	V	VCC= 5.0V
V_{IH}	Input HIGH Voltage	2.00	VCC+0.3	V	VCC= 5.0V
V_{OL}	Output LOW Voltage		0.45	V	VCC= 5.0V
V_{OH}	Output HIGH Voltage	2.40		V	VCC= 5.0V
I_{CC}	Operating Current, VCC_R=5.0V				
	Sleep Mode		0.20	mA	
	Operating Current		30.00	mA	
I_{CC}	Operating Current, VCC_R=3.3V				
	Sleep Mode		0.20	mA	
	Operating Current		30.00	mA	
I_{LI}	Input Leakage Current		±10	µA	
I_{LO}	Output Leakage Current		±10	µA	

1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

7.2 AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

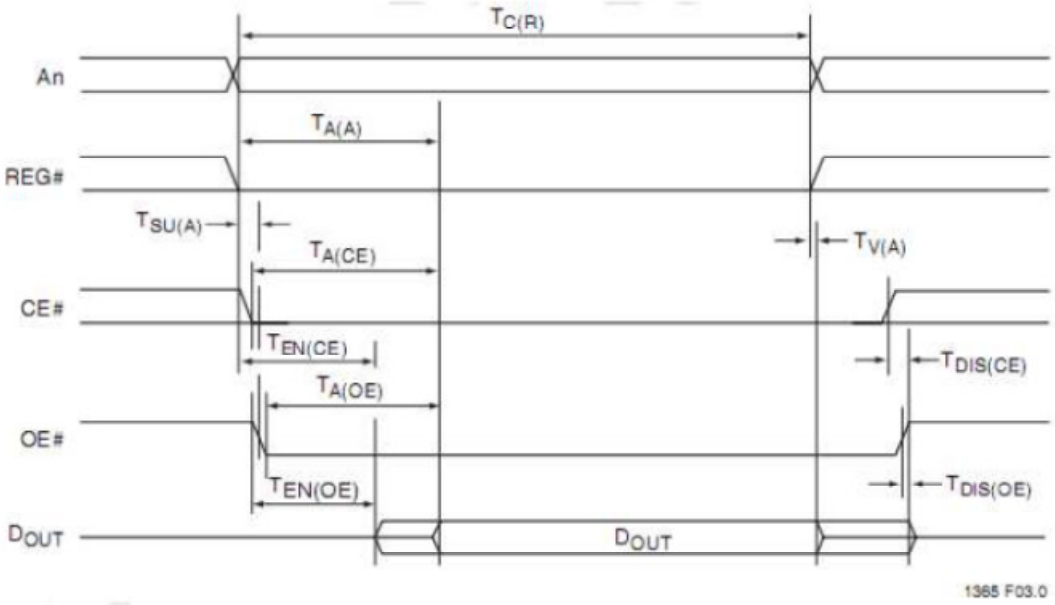
Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

7.2.1 Attribute Memory Read and Write Specification

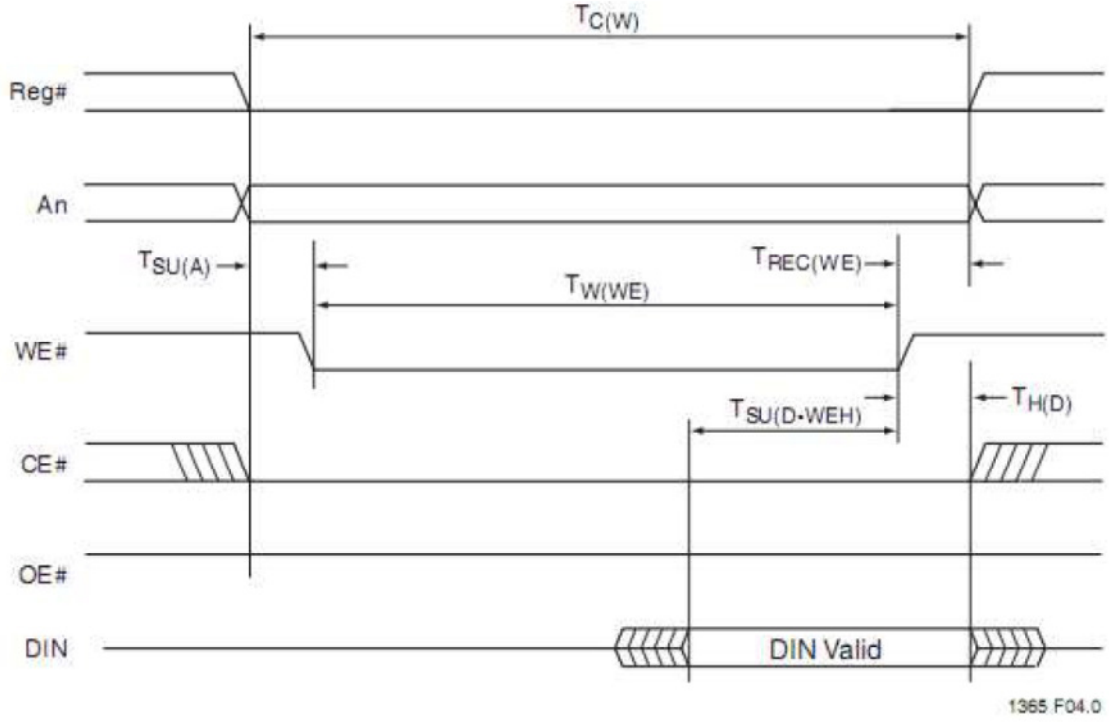
The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in the table below.

Table 7-4 Attribute Memory Read and Write Timing

Symbol	Parameter	Min	Max	Units	Notes
t_{cR}	Read Cycle Time	250		ns	
$t_{a(A)}$	Address Access Time		250	ns	
$t_{a(CE)}$	Card Enable Access Time		250	ns	
$t_{a(OE)}$	Output Enable Access Time		125	ns	
$t_{dis(CE)}$	Output Disable time from CE		100	ns	
$t_{dis(OE)}$	Output Disable time from OE		100	ns	
$t_{en(CE)}$	Output Enable time from CE	5		ns	
$t_{en(OE)}$	Output Enable time from OE	5		ns	
$t_{V(A)}$	Data valid time from address change	0		ns	
$t_{su(A)}$	Address Setup Time	30		ns	
$t_{h(A)}$	Address Hold Time	20		ns	
$t_{su(CE)}$	Card Enable Setup Time	0		ns	
$t_{h(CE)}$	Card Enable Hold Time	20		ns	
t_{cW}	Write Cycle Time	250		ns	
$t_{w(WE)}$	Write Pulse Time	150		ns	
$t_{su(A-WEH)}$	Address setup time for WE	180		ns	
$t_{su(CE-WEH)}$	Card Enable setup time for WE	180		ns	
$t_{su(D-WEH)}$	Data setup time for WE	80		ns	
$t_{h(D)}$	Data hold time	30		ns	
$t_{dis(WE)}$	Output disable time from WE		100	ns	
$t_{en(WE)}$	Output enable time from WE	5		ns	
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns	
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns	



Attribute Memory Read Timing Diagram

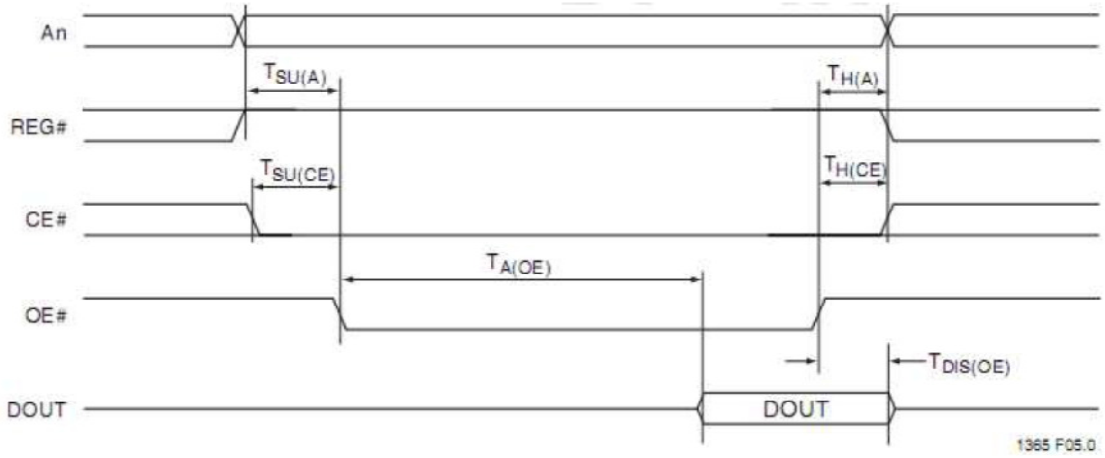


Configuration Register (Attribute Memory) Write Timing Diagram

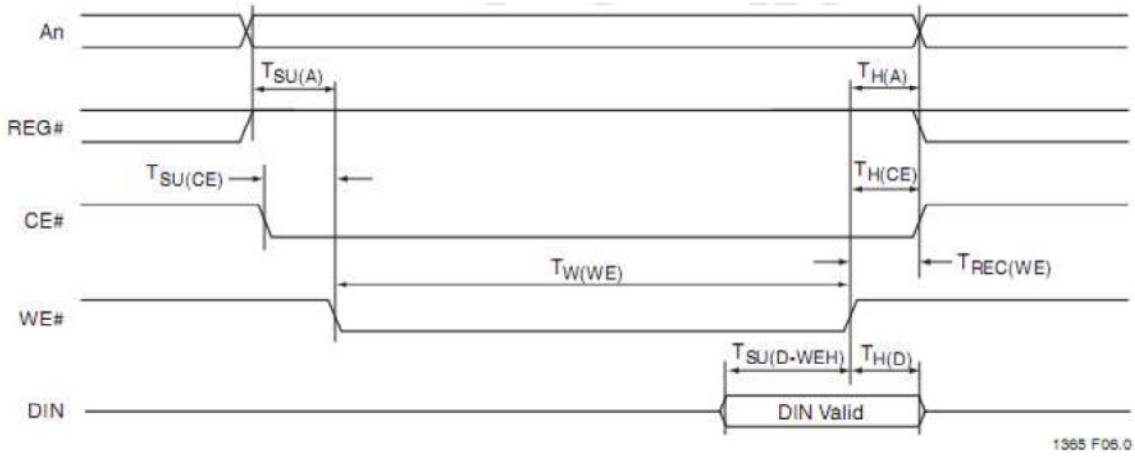
7.2.2 Common Memory Read and Write Timing Specification

Table 7-5 Common Memory Read and Write Timing

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	150		ns
$t_{a(A)}$	Address Access Time		150	ns
$t_{a(CE)}$	Card Enable Access Time		150	ns
$t_{a(OE)}$	Output Enable Access Time		75	ns
$t_{dis(CE)}$	Output Disable time from CE		75	ns
$t_{dis(OE)}$	Output Disable time from OE		75	ns
$t_{en(CE)}$	Output Enable time from CE	5		ns
$t_{en(OE)}$	Output Enable time from OE	5		ns
$t_{V(A)}$	Data valid time from address change	0		ns
$t_{su(A)}$	Address Setup Time	20		ns
$t_{h(A)}$	Address Hold Time	20		ns
$t_{su(CE)}$	Card Enable Setup Time	0		ns
$t_{h(CE)}$	Card Enable Hold Time	20		ns
t_{cW}	Write Cycle Time	150		ns
$t_{w(WE)}$	Write Pulse Time	80		ns
$t_{su(A-WEH)}$	Address setup time for WE	100		ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE	100		ns
$t_{su(D-WEH)}$	Data setup time for WE	50		ns
$t_{h(D)}$	Data hold time	20		ns
$t_{rec(WE)}$	Write recovery time	20		ns
$t_{dis(WE)}$	Output disable time from WE		75	ns
$t_{en(WE)}$	Output enable time from WE	5		ns
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns



Common Memory Read Timing Diagram

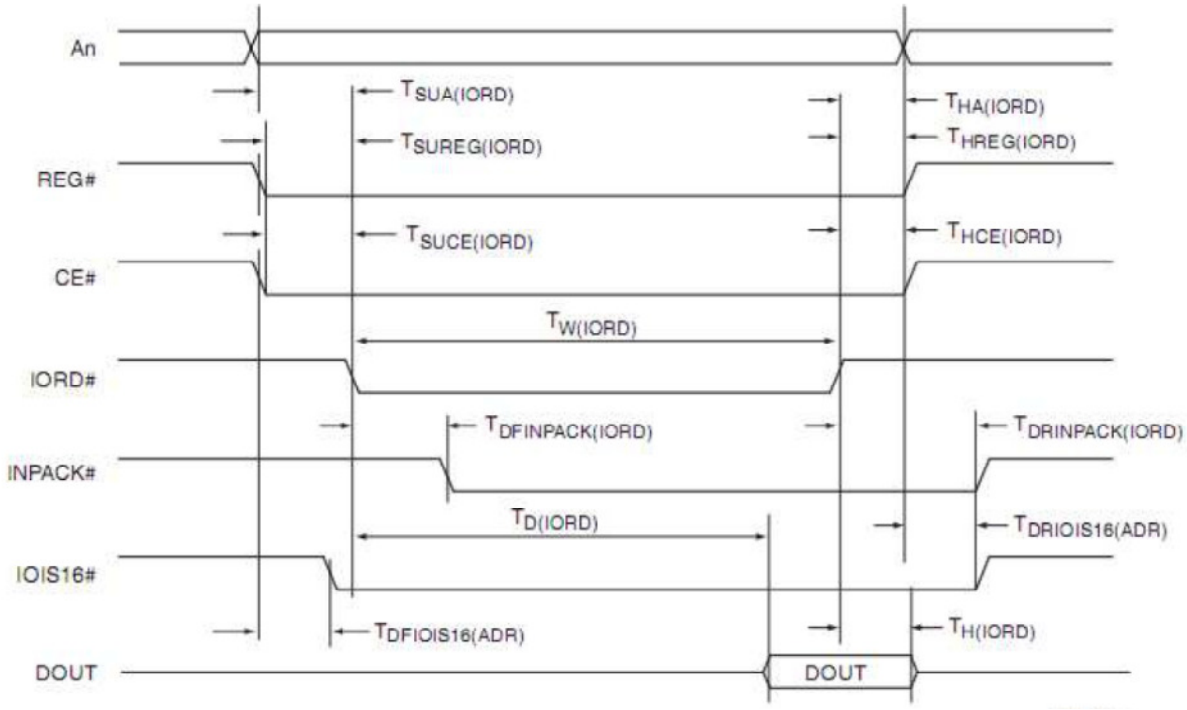


Common Memory Write Timing Diagram

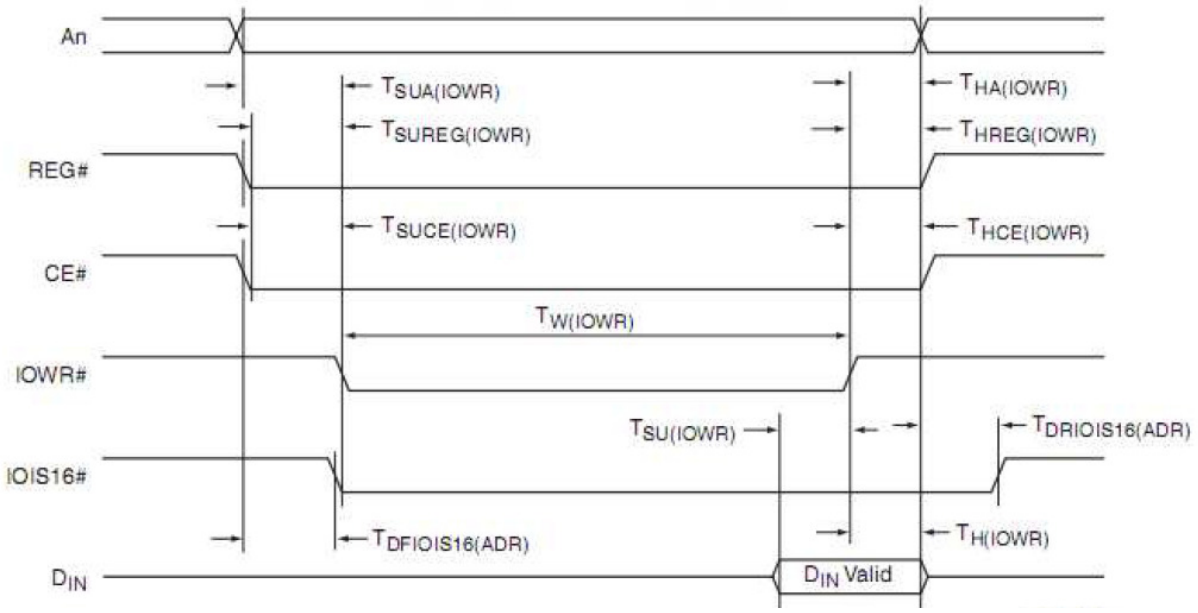
7.2.3 I/O Read and Write Timing Specification

Table 7-5 I/O Read and Write Timing

Symbol	Parameter	Min	Max	Units
$t_{d(IORD)}$	Data Delay after IORD		100	ns
$t_{h(IORD)}$	Data Hold following IORD	0		ns
$t_{w(IORD)}$	IORD pulse width	165		ns
$t_{suA(IORD)}$	Address setup time for IORD	70		ns
$t_{hA(IORD)}$	Address hold time for IORD	20		ns
$t_{suCE(IORD)}$	Card Enable setup time for IORD	5		ns
$t_{hCE(IORD)}$	Card Enable hold time from IORD	20		ns
$t_{suREG(IORD)}$	REG setup time for IORD	5		ns
$t_{hREG(IORD)}$	REG Hold time from IORD	0		ns
$t_{dfl\ NP(IORD)}$	INPACK delay falling from IORD	0	45	ns
$t_{drlNP(IORD)}$	INPACK delay rising from IORD		45	ns
$t_{dfl\ O16(IORD)}$	IOIS16 delay falling from address		35	ns
$t_{drlO16(IORD)}$	IOIS16 delay rising from address		35	ns
$t_{su(IOWR)}$	Data setup time for IOWR	60		ns
$t_{h(IOWR)}$	Data hold time from IOWR	30		ns
$t_{w(IOWR)}$	IOWR pulse width	165		ns
$t_{suA(IOWR)}$	Address setup time for IOWR	70		ns
$t_{hA(IOWR)}$	Address hold time from IOWR	20		ns
$t_{suCE(IOWR)}$	Card Enable setup time for IOWR	5		ns
$t_{hCE(IOWR)}$	Card Enable hold time from IOWR	20		ns
$t_{suREG(IOWR)}$	REG setup time for IOWR	5		ns
$t_{hREG(IOWR)}$	REG hold time from IOWR	0		ns



I/O Read Timing Diagram



I/O Write Timing Diagram

7.2.4 TrueIDE Read and Write Timing Specification

Table 7-6 TrueIDE Read and Write Timing

Symbol	Parameter	Min	Max	Units
t_{cR}	Cycle time	120		ns
t_{suA}	Address setup time for IORD/IOWR	25		ns
t_{hA}	Address hold time from IORD/IOWR	10		ns
t_{w}	IORD/IORW recovery time	70		ns
t_{rec}	IORD/IORW recovery time	25		ns
$t_{suD(IORD)}$	Data setup time for IORD	20		ns
$t_{hD(IORD)}$	Data hold time for IORD	5		ns
$t_{dis(IORD)}$	Output disable time from IORD		30	ns
$t_{suD(IOWR)}$	Data setup time for IOWR	20		ns
$t_{hD(IOWR)}$	Data hold following IOWR	10		ns

8. Physical Characteristics

8.1 Dimensions

TABLE 8-1: Type II PCMCIA physical specification

Length:	85.6 +/- 0.20mm (3.370”)
Width:	54.0 +/- 0.10mm (2.126”)
Thickness (Including Label Area):	5.0mm+/-0.10mm (0.197”.)

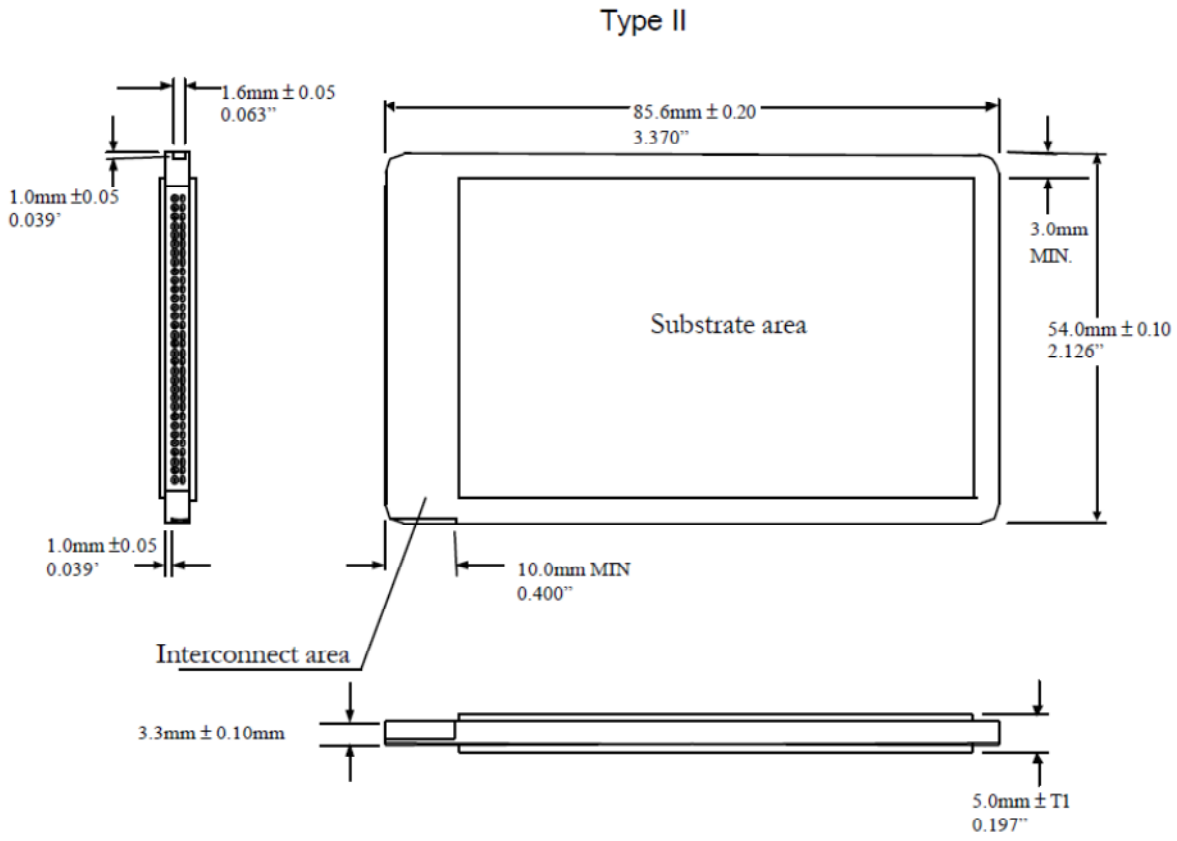
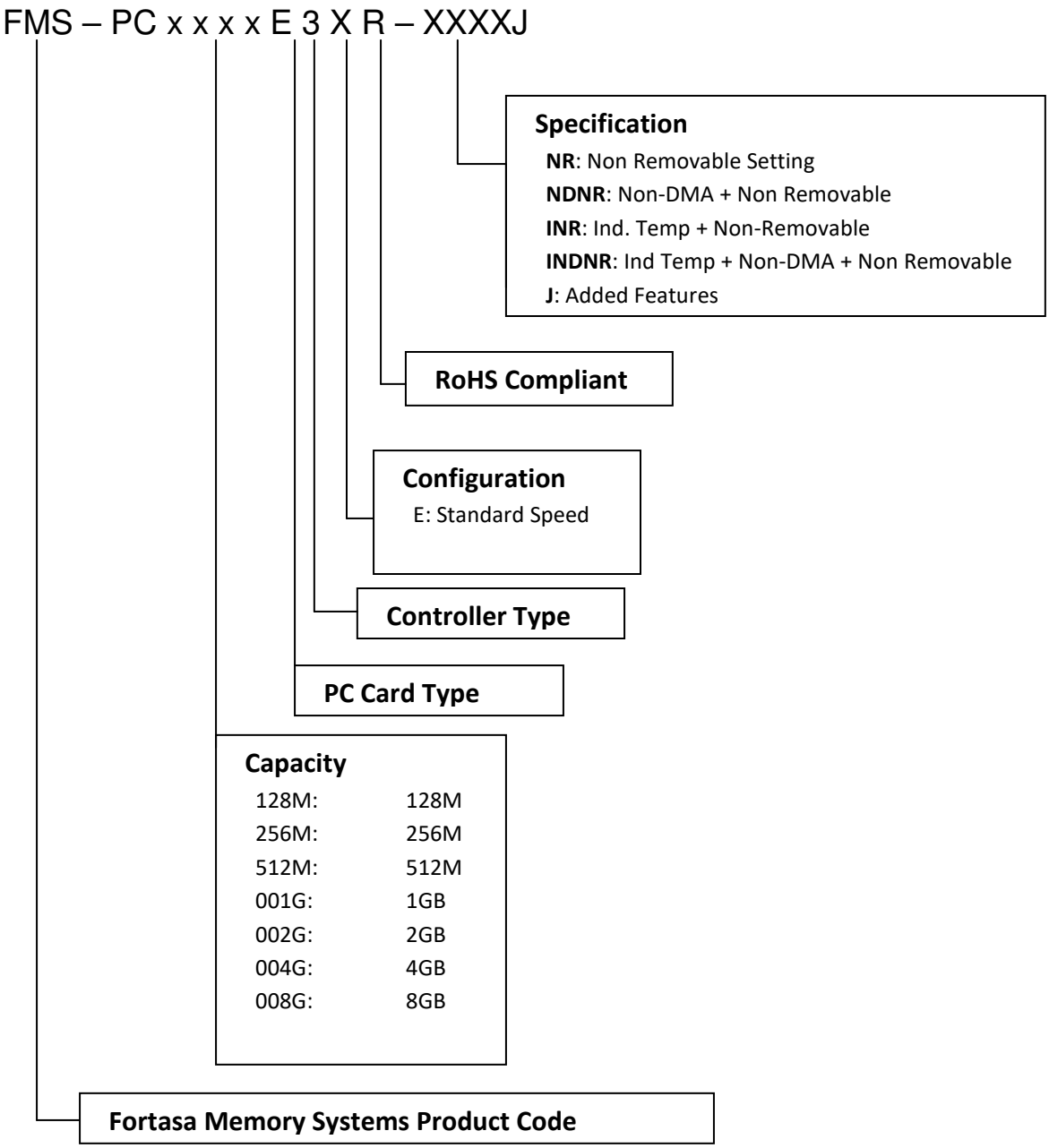


FIGURE 8-1: Physical dimension

9. Product Ordering Information

9.1 Product Code Designations



9.2 Valid Combinations

Standard Temperature

Capacity	Model Number
128M	FMS-PC128ME3ER-xxxxJ
256M	FMS-PC256ME3ER-XXXXJ
512M	FMS-PC512ME3ER-XXXXJ
1GB	FMS-PC001GE3ER-XXXXJ
2GB	FMS-PC002GE3ER-XXXXJ
4GB	FMS-PC004GE3ER-XXXXJ
8GB	FMS-PC008GE3ER-XXXXJ

Industrial Temperature

Capacity	Model Number
128M	FMS-PC128ME3ER-IxxxxJ
256M	FMS-PC256ME3ER-IXXXXJ
512M	FMS-PC512ME3ER-IXXXXJ
1GB	FMS-PC001GE3ER-IXXXXJ
2GB	FMS-PC002GE3ER-IXXXXJ
4GB	FMS-PC004GE3ER-IXXXXJ
8GB	FMS-PC008GE3ER-IXXXXJ

10. Revision History

Revision	Date	Description	Comments
1.0	02/11/2010	Initial Release	
1.1	10/05/2012	Added Drive ID Table	
1.2	2/06/2014	Updated Performance Specification	